7. SED1560 Series

Contents

OVERVIEW

The SED1560 series is a single-chip LCD driver for dot-matrix liquid crystal displays. It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip 166 × 65-bit RAM.

The SED1560 features 167 common and segment outputs to drive either a 65 × 102-pixel (SED1560) display (4 rows × 6 columns with 16 × 16-pixel characters) or a 33 × 134-pixel (SED1561) display (2 rows × 8 columns with 16 × 16-pixel characters) or a 17 × 150-pixel (SED1562) display (1 row × 9 columns with 16 × 16 characters). In addition, two SED1560s can be connected together to drive a 65 × 268-pixel graphics display panel.

The SED 1560 series can read and write RAM data with the minimum current consumption as it does not require any external operation clock. Also, it has a built-in LCD power supply featuring the very low current consumption and, therefore, the display system of a high-performance but handy instrument can be realized by use of the minimum current consumption and LSI chip configuration.

The SED 1560 Series has the SED1560, SED1561 and SED1562 available according to the duty.

FEATURES

- Wide variety of duty and display areas

Model	Duty	LCD bias	Single-chip display area
SED1560	1/65 1/64 1/49 1/48	1/9 1/7	65 × 102 64 × 102 49 × 102 48 × 102
SED1561	1/33 1/32 1/25 1/24	1/7 1/5	33 × 134 32 × 134 25 × 134 24 × 134
SED1562	1/17 1/16	1/5	17 × 150 16 × 150

Note: The LCD bias is obtained if the built-in power supply is used.

- On-chip 166 × 65-bit display RAM
- Direct relationship between RAM bits and display pixels.
- High speed Interfaces to 6800- and 8080-series microprocessors
- Selectable 8-bit parallel/serial interface
- Many command functions
- On-chip LCD power circuit including DC/DC voltage converter, voltage regulator and voltage followers.
- On-Chip Contrast control.
- Two types of V_{REG} (Built-in power supply regulator temperature gradient).
- Type1 (SED156∗D$_O$∗, SED156∗D$_A$∗)...–0.2%/˚C
- Type2 (SED1560D$_E$∗)...0.00%/˚C
- On-chip oscillator
- Ultra low power consumption
- Power Supply
  $V_{DD} – V_{SS}$ –2.4 V to –6.0 V
  $V_{DD} – V_5$ –3.5 V to –16.0 V
- Ta = –30 to 85°C
- CMOS process
- TCP, QTCP
- The system is not designed against the radio activity.

PAD LAYOUT

	Chip size	:	8.08 × 5.28 mm
	Pad pitch	:	100 µm (Min.)
	Chip thickness	:	625 µm
		:	300 µm (Al-pad)
• Au-Bump			
	Bump size A	:	103 µm × 95 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
	Bump size B	:	69 µm × 95 µm (Typ.) (other then the above)
	Bump hight	:	23 µm (Typ.)
• Al-pad			
	Pad size A	:	111 µm × 102 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
	Bump size B	:	77 µm × 99 µm (Typ.) (Other then the above)

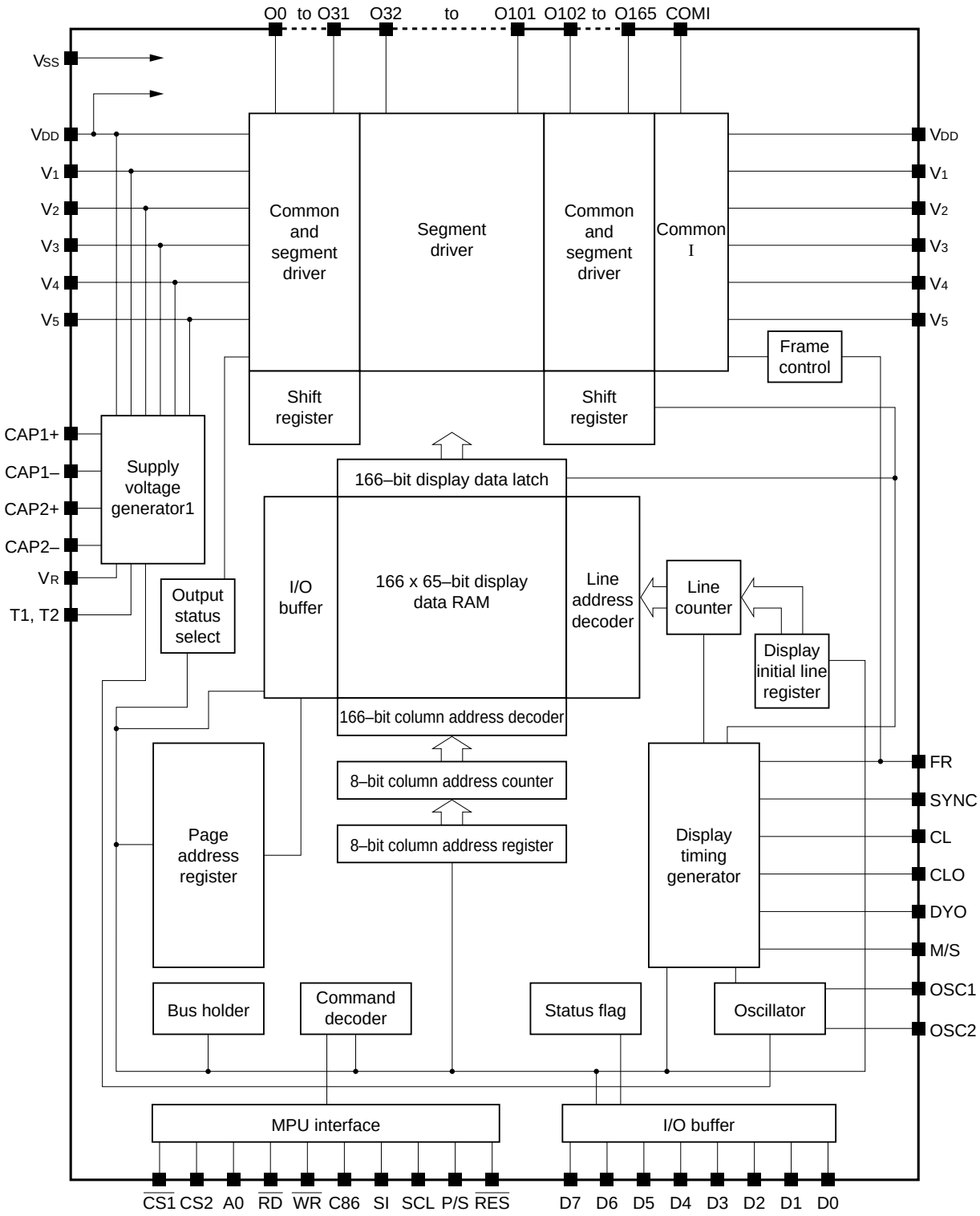
SED1560SERIES

PAD Center Coordinates

Unit : μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_5	3640	2487	55	05	-3887	1794	109	059	-2411	-2487	163	0113	2989	-2487
2	V_4	3489	2487	56	06	-3887	1694	110	060	-2311	-2487	164	0114	3089	-2487
3	V_3	3339	2487	57	07	-3887	1594	111	061	-2211	-2487	165	0115	3189	-2487
4	V_2	3188	2487	58	08	-3887	1494	112	062	-2111	-2487	166	0116	3289	-2487
5	V_1	3037	2487	59	09	-3887	1394	113	063	-2011	-2487	167	0117	3389	-2487
6	V_{DD}	2889	2487	60	010	-3887	1294	114	064	-1911	-2487	168	0118	3489	-2487
7	M/S	2755	2487	61	011	-3887	1194	115	065	-1811	-2487	169	0119	3589	-2487
8	$\overline{RES}$	2604	2487	62	012	-3887	1094	116	066	-1711	-2487	170	0120	3689	-2487
9	SCL	2453	2487	63	013	-3887	994	117	067	-1611	-2487	171	0121	3887	-2206
10	SI	2302	2487	64	014	-3887	894	118	068	-1511	-2487	172	0122	3887	-2106
11	P/S	2151	2487	65	015	-3887	794	119	069	-1411	-2487	173	0123	3887	-2006
12	$\overline{CS1}$	2001	2487	66	016	-3887	694	120	070	-1311	-2487	174	0124	3887	-1906
13	CS2	1850	2487	67	017	-3887	594	121	071	-1211	-2487	175	0125	3887	-1806
14	C86	1699	2487	68	018	-3887	494	122	072	-1111	-2487	176	0126	3887	-1706
15	A0	1548	2487	69	019	-3887	394	123	073	-1011	-2487	177	0127	3887	-1606
16	$\overline{WR}$	1397	2487	70	020	-3887	294	124	074	-911	-2487	178	0128	3887	-1506
17	$\overline{RD}$	1247	2487	71	021	-3887	194	125	075	-811	-2487	179	0129	3887	-1406
18	V_{SS}	1077	2487	72	022	-3887	94	126	076	-711	-2487	180	0130	3887	-1306
19	D0	945	2487	73	023	-3887	-6	127	077	-611	-2487	181	0131	3887	-1206
20	D1	794	2487	74	024	-3887	-106	128	078	-511	-2487	182	0132	3887	-1106
21	D2	643	2487	75	025	-3887	-206	129	079	-411	-2487	183	0133	3887	-1006
22	D3	493	2487	76	026	-3887	-306	130	080	-311	-2487	184	0134	3887	-906
23	D4	342	2487	77	027	-3887	-406	131	081	-211	-2487	185	0135	3887	-806
24	D5	191	2487	78	028	-3887	-506	132	082	-111	-2487	186	0136	3887	-706
25	D6	40	2487	79	029	-3887	-606	133	083	-11	-2487	187	0137	3887	-606
26	D7	-111	2487	80	030	-3887	-706	134	084	89	-2487	188	0138	3887	-506
27	DYO	-261	2487	81	031	-3887	-806	135	085	189	-2487	189	0139	3887	-406
28	CLO	-412	2487	82	032	-3887	-906	136	086	289	-2487	190	0140	3887	-306
29	SYNC	-563	2487	83	033	-3887	-1006	137	087	389	-2487	191	0141	3887	-206
30	FR	-714	2487	84	034	-3887	-1106	138	088	489	-2487	192	0142	3887	-106
31	CL	-865	2487	85	035	-3887	-1206	139	089	589	-2487	193	0143	3887	-6
32	OSC2	-1015	2487	86	036	-3887	-1306	140	090	689	-2487	194	0144	3887	94
33	OSC1	-1166	2487	87	037	-3887	-1406	141	091	789	-2487	195	0145	3887	194
34	T2	-1317	2487	88	038	-3887	-1506	142	092	889	-2487	196	0146	3887	294
35	T1	-1468	2487	89	039	-3887	-1606	143	093	989	-2487	197	0147	3887	394
36	V_{SS}	-1638	2487	90	040	-3887	-1706	144	094	1089	-2487	198	0148	3887	494
37	CAP1+	-1789	2487	91	041	-3887	-1806	145	095	1189	-2487	199	0149	3887	594
38	CAP1-	-1939	2487	92	042	-3887	-1906	146	096	1289	-2487	200	0150	3887	694
39	CAP2+	-2090	2487	93	043	-3887	-2006	147	097	1389	-2487	201	0151	3887	794
40	CAP2-	-2241	2487	94	044	-3887	-2106	148	098	1489	-2487	202	0152	3887	894
41	V_{OUT}	-2392	2487	95	045	-3887	-2206	149	099	1589	-2487	203	0153	3887	994
42	V_5	-2543	2487	96	046	-3711	-2487	150	0100	1689	-2487	204	0154	3887	1094
43	V_R	-2674	2487	97	047	-3611	-2487	151	0101	1789	-2487	205	0155	3887	1194
44	V_{DD}	-2844	2487	98	048	-3511	-2487	152	0102	1889	-2487	206	0156	3887	1294
45	V_1	-2995	2487	99	049	-3411	-2487	153	0103	1989	-2487	207	0157	3887	1394
46	V_2	-3146	2487	100	050	-3311	-2487	154	0104	2089	-2487	208	0158	3887	1494
47	V_3	-3297	2487	101	051	-3211	-2487	155	0105	2189	-2487	209	0159	3887	1594
48	V_4	-3447	2487	102	052	-3111	-2487	156	0106	2289	-2487	210	0160	3887	1694
49	V_5	-3598	2487	103	053	-3011	-2487	157	0107	2389	-2487	211	0161	3887	1794
50	00	-3887	2294	104	054	-2911	-2487	158	0108	2489	-2487	212	0162	3887	1894
51	01	-3887	2194	105	055	-2811	-2487	159	0109	2589	-2487	213	0163	3887	1994
52	02	-3887	2094	106	056	-2711	-2487	160	0110	2689	-2487	214	0164	3887	2094
53	03	-3887	1994	107	057	-2611	-2487	161	0111	2789	-2487	215	0165	3887	2194
54	04	-3887	1894	108	058	-2511	-2487	162	0112	2889	-2487	216	COMI	3887	2294

BLOCK DIAGRAM



PIN DESCRIPTION

Power Supply

Number of pins	I/O	Name	Description
2	Supply	V_{DD}	5V supply. Common to MPU power supply pin V_{CC}.
2	Supply	V_{SS}	Ground
11	Supply	V_1 to V_5	LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be determined on a V_{DD}-basis so as to satisfy the following relationship. The voltages must satisfy the following relationship. $V_{DD} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$. When master mode selects, these voltages are generated on-chip.

	SED1560D0B	SED1560DAB SED1561D0B	SED1561DAB SED1562D0B
V_1	1/9 V_5	1/7 V_5	1/5 V_5
V_2	2/9 V_5	2/7 V_5	2/5 V_5
V_3	7/9 V_5	5/7 V_5	3/5 V_5
V_4	8/9 V_5	6/7 V_5	4/5 V_5

LCD Driver Supplies

Number of pins	I/O	Name	Description
1	O	CAP1+	DC/DC voltage converter capacitor 1 positive connection
1	O	CAP1–	DC/DC voltage converter capacitor 1 negative connection
1	O	CAP2+	DC/DC voltage converter capacitor 2 positive connection
1	O	CAP2–	DC/DC voltage converter capacitor 2 negative connection
1	I/O	V_{OUT}	DC/DC voltage converter output
1	I	V_R	Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.
2	I	T1, T2	Liquid crystal power control terminals

T1	T2	Boosting circuit	Voltage regulation circuit	V/F circuit
L	L	Valid	Valid	Valid
L	H	Valid	Valid	Valid
H	L	Invalid	Valid	Valid
H	H	Invalid	Invalid	Valid

Microprocessor Interface

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>8</td><td>I/O</td><td>D0 to D7</td><td>Data inputs/outputs</td></tr>
<tr><td>1</td><td>I</td><td>A0</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
When LOW, the data on D0 to D7 is control data.
When HIGH, the data on D0 to D7 is display data.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RES}$</td><td>Reset input. System is reset and initialized when LOW.</td></tr>
<tr><td>2</td><td>I</td><td>$\overline{CS1}$, CS2</td><td>Chip select inputs. Data input/output is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RD}$ (E)</td><td>Read enable input. See note. 1</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>Write enable input. See note. 2</td></tr>
<tr><td>1</td><td>I</td><td>C86</td><td>Microprocessor interface select input. LOW when interfacing to 8080-series. HIGH when interfacing to 6800-series.</td></tr>
<tr><td>1</td><td>I</td><td>SI</td><td>Serial data input</td></tr>
<tr><td>1</td><td>I</td><td>SCL</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td></tr>
<tr><td>1</td><td>I</td><td>P/S</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating mode</th><th>Chip select</th><th>Data/command</th><th>Data input/ output</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td></tr>
</table>

Note 1
When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.

Note 2
When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, It will be read mode when $\overline{WR}$ is high and It will be write mode when $\overline{WR}$ is LOW.

Oscillator and Timing Control

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>I</td><td>OSCI</td><td>Connecting pins for feedback resistors of the built-in oscillator
When M/S = “H”: Connect oscillator resistor Rf to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td></tr>
<tr><td>2</td><td>I/O</td><td>OSC2</td><td>When M/S = “L”: The OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the CL pin to the VSS level when using the internal oscillator circuit as the display clock.</td></tr>
<tr><td>1</td><td>I</td><td>CL</td><td>Display clock input. The line counter increments on the rising edge of CL and the display pattern is output on the falling edge. When use external display clock, OSC1 = “H”, OSC2 = “L” and reset this LSI by $\overline{RES}$ pin.</td></tr>
<tr><td>1</td><td>O</td><td>CLO</td><td>Display clock output. When using the master operation, the clock signal is output on this pin. Connect CLO to YSCL on the common driver.</td></tr>
<tr><td>1</td><td>I</td><td>M/S</td><td>Master/slave select input. Master makes some signals for display, and slave gets them. This is for display syncronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating mode</th><th>Internal oscillator</th><th>Power supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156XDOB</td><td>Low</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note
I = input mode
O = output mode</td></tr>
<tr><td>1</td><td>I/O</td><td>FR</td><td>LCD AC drive signal input/output. If the SED1560 series MPU’s are used in master and slave configuration, this pin must be connected to each FR pin. Also when the SED1560 series is used as the master MPU, this pin must be connected to the FR pin of the common driver. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>I/O</td><td>SYNC</td><td>Display sync input/output. If the SED1560 series MPU’s are used in master and slave configuration, this pin must be connected to each SYNC pin. Output is selected when M/S is HIGH, and Input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>O</td><td>DYO</td><td>Start-up output for common driver. Connect to DIO of the common driver.</td></tr>
</table>

LCD Driver Outputs

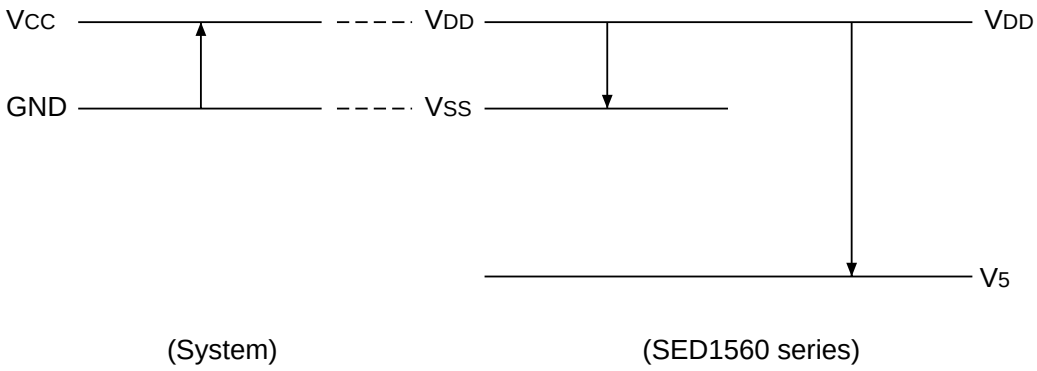
<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>166</td><td>O</td><td>O0 to O165</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.

For segment outputs, the ON voltage level is given as shown in the following table.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">LCD ON voltage</th></tr>
<tr><th>Normal display</th><th>Inverse display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table.
<table>
<tr><th>Scan data</th><th>FR</th><th>LCD ON voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>HIGH</td><td>V_1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>HIGH</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>1</td><td>O</td><td>COMI</td><td>LCD driver common output. Common outputs when the “DUTY + 1” command is executed are as follows:
<table>
<tr><th></th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>SED1560
SED1561
SED1562</td><td>COM64, COM48
COM32, COM24
COM16</td><td>V_1 or V_4
V_1 or V_4
V_1 or V_4</td></tr>
</table>
Common output special for the indicator.</td></tr>
</table>

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 +0.03	V
Supply voltage range (2) (DC/DC When in use)		–6.0 to 0.3 (when triple boosting)	
Driver supply voltage range (1)	V_5	–18.0 to 0.3	V
Driver supply voltage range (2)	V_1, V_2, V_3, V_4	V_5 to 0.3	V
Input voltage range	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage range	Vo	V_{SS} –0.3 to 0.3	V
Operating temperature range	Topr	–30 to 85	deg. C
Storage temperature range (TCP)	Tstr	–55 to 100	deg. C



Notes: 1. The voltages shown are based on V_{DD} = 0 V.
2. Always keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ for voltages V_1, V_2, V_3 and V_4.
3. If LSIs are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. A guarantee on operating temperature below –30°C may be studied individually.

DC Characteristics

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommend-ed operation	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Operational				–6.0		–2.4		*1
Operating voltage (2)	Operational	V_5			–16.0		–4.0	V	V_5 *2
	Operational	V_1, V_2			0.4 × V_5		V_{DD}	V	V_1, V_2
	Operational	V_3, V_4			V_5		0.6 × V_5	V	V_3, V_4
High-level input voltage		V_{IHC1}			0.3 × V_{SS}		V_{DD}	V	*3
		V_{IHC2}			0.15 × V_{SS}		V_{DD}		*4
		V_{IHC1}	V_{SS} = –2.7 V		0.3 × V_{SS}		V_{DD}		*3
		V_{IHC2}	V_{SS} = –2.7 V		0.2 × V_{SS}		V_{DD}		*4
Low-level input voltage		V_{ILC1}			V_{SS}		0.7 × V_{SS}	V	*3
		V_{ILC2}			V_{SS}		0.85 × V_{SS}		*4
		V_{ILC1}	V_{SS} = –2.7 V		V_{SS}		0.7 × V_{SS}		*3
		V_{ILC2}	V_{SS} = –2.7 V		V_{SS}		0.8 × V_{SS}		*4
High-level output voltage		V_{OHC1}		I_{OH} = –1 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}		I_{OH} = –120 µA	0.2 × V_{SS}		V_{DD}		OSC2
		V_{OHC1}	V_{SS} = –2.7 V	I_{OH} = –0.5 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}	V_{SS} = –2.7 V	I_{OH} = –50 µA	0.2 × V_{SS}		V_{DD}		OSC2
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}		I_{OL} = 120 µA	V_{SS}		0.8 × V_{SS}		OSC2
		V_{OLC1}	V_{SS} = –2.7 V	I_{OL} = 0.5 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}	V_{SS} = –2.7 V	I_{OL} = 50 µA	V_{SS}		0.8 × V_{SS}		OSC2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0		1.0	µA	*6
Output leakage current		I_{LO}			–3.0		3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V_5 = –14.0 V		2.0	3.0	KΩ	O0 to O166
				V_5 = –8.0 V		3.0	4.5		*8
Static power consumption		I_{SSQ}				0.00	5.0	µA	V_{SS}
		I_{5Q}	V_5 = –18.0V			0.01	15.0	µA	V_5
Input terminal capacity		C_{IN}	Ta = 25°C	f=1MHz		5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	R_f=1 MΩ	V_{SS} = –5V	15	18	22	kHz	*9
			±2%	V_{SS} = –2.7V	11	16	21		

Reset time	t_R		1.0			µs	*10
Reset "L" pulse width	t_{RW}		1.0			µs	*11

Built-in power circuit	Input voltage	V_{SS}		–6.0		–2.4	V	*12
	Amplified out-put voltage	V_{OUT}	when triple boosting	–18.0			V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}		–16.0		–6.0	V	V_{OUT}
	Voltage regulutor operation voltage	V_5 ①	Supplied to SED1560D$_{OB}$	–16.0		–6.0	V	*13
		V_5 ②	Supplied to SED1561D$_{OB}$	–16.0		–5.0	V	
		V_5 ③	Supplied to SED1561D$_{AB}$	–16.0		–4.0	V	
		V_5 ④	Supplied to SED1562D$_{OB}$	–16.0		–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.35	–2.5	–2.65	V	

*V_{SS} = –2.4V is on the same basis as V_{SS} = –2.7V.

* See the 4-12 page for details.

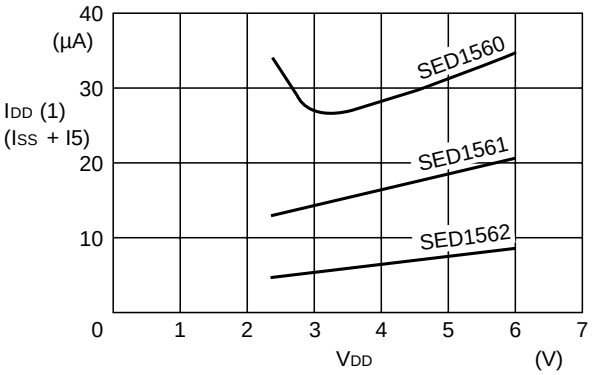
When dynamic current consumption (I) is displaye; the built-in power circuit is on and T1 = T2 = Low.

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SED1560	I_{DD} (1)	V_5 = –12.5 V; 3 times amplified		169	340	µA	*16
SED1561		V_5 = –8.0 V ; 3 times amplified		124	250	µA	
SED1562		V_5 = –6.0 V ; 2 times amplified		53	110	µA	
		V_{SS} = –2.7 V; 3 times amplified V_5 = –6.0 V		66	130	µA	

Typical current consumption characteristics

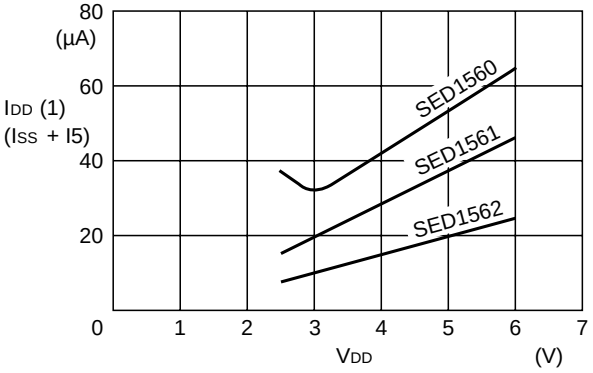
- Dynamic current consumption (I), if an external clock and an external power supply are used.



Conditions: The built-in power supply is off but the external one is used.
SED1560 $V_5 – V_{DD}$ = –12.5 V
SED1561 $V_5 – V_{DD}$ = –8.0 V
SED1562 $V_5 – V_{DD}$ = –6.0 V
External clock:
SED1560 f_{CL} = 4 kHz
SED1561 f_{CL} = 2 kHz
SED1562 f_{CL} = 1 kHz

Remarks: *14

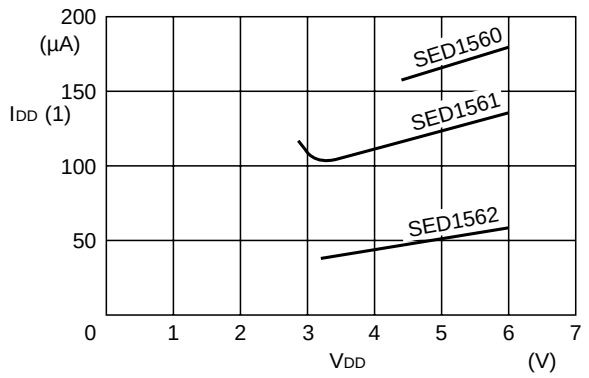
- Dynamic current consumption (I), if the built-in oscillator and the external power supply are used.



Conditions: The built-in power supply is off but the external one is used.
SED1560 $V_5 – V_{DD}$ = –12.5 V
SED1561 $V_5 – V_{DD}$ = –8.0 V
SED1562 $V_5 – V_{DD}$ = –6.0 V
Internal oscillation:
SED1560 R_f = 1 MΩ
SED1561 R_f = 1 MΩ
SED1562 R_f = 1 MΩ

Remarks: *15

- Dynamic current consumption (I), if the built-in power supply is used.



Conditions: The built-in power supply is on and T1 = T2 = Low.

SED1560 $V_5 - V_{DD}$ = –12.5 V; 3 times amplified

SED1561 $V_5 - V_{DD}$ = –8.0 V; 3 times amplified

SED1562 $V_5 - V_{DD}$ = –6.0 V; 2 times amplified

Internal oscillation:

SED1560 R_f = 1 MΩ

SED1561 R_f = 1 MΩ

SED1562 R_f = 1 MΩ

Remarks: *16

Notes: *1. Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.

*2. The operating voltage range of the V_{SS} and V_5 systems (see Figure 11).
The operating voltage range is applied if an external power supply is used.

*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 and T2.

*4. Pins CL, SCL, and $\overline{RES}$

*5. Pins D0 to D7, FR, SYNC, CL0, and DY0

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.

*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.

*8. The resistance when the 0.1-volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).
R ON = 0.1 V/ΔI
(ΔI is the current that flows when 0.1 VDC is applied during power-on.)

*9. The relationship between the oscillation frequency, frame and Rf value (see Figure 10).

10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the SED156 is usually operable after "tr" time.

*11. Specifies the minimum pulse width of $\overline{RES}$" signal. The Low pulse greater than "t_{RW}" must be entered for reset.

*12. If the voltage is amplified three times by the built-in power circuit, the primary power V_{SS} must be used within the input voltage range.

*13. The V_5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.

*14, 15, 16 Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.
The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the SED1560D_{0B} is set to 1/64 duty, the SED1561D_{0B} is set to 1/32 duty, and the SED1562D_{0B} is set to 1/16 duty.

*14. Applied if an external clock is used and if not accessed by the MPU.

*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.

*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU. Measuring conditions: C1 = 4.7 μF, C2 = 0.47 μF, Ra + Rb = 2 MΩ
This includes the current that flows through the voltage regulator resistor (Ra + Rb = 2 MΩ). If the built-in power circuit is used, the current consumption is equal to the current of V_{SS} power.

Oscillator frequency vs. frame vs. Rf [SED156*D0B]

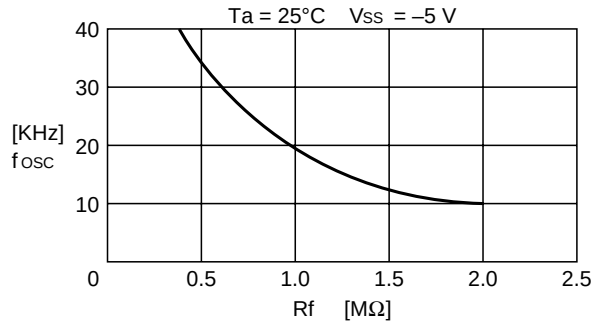


Figure 10 (a)

External clock (f_{CL}) vs. frame [SED156*D*B]

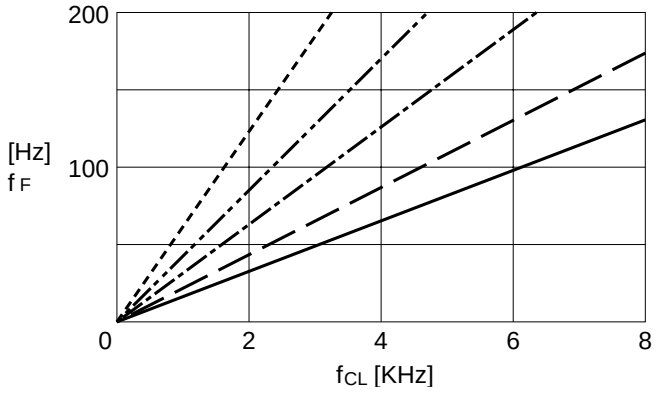


Figure 10 (b)

The relationship between oscillator frequency f_{OSC} and LCD frame frequency f_F is obtained from the following expression.

	Duty	f_F
SED1560	1/64	$f_{OSC}/256$
	1/48	$f_{OSC}/192$
SED1561	1/32	$f_{OSC}/256$
	1/24	$f_{OSC}/192$
SED1562	1/16	$f_{OSC}/256$

(f_F indicates not f_F signal cycle but cycle of LCD AC.)

duty 1/64 SED1560
duty 1/48
duty 1/32 SED1561
duty 1/24
duty 1/16 SED1562

Operating voltage range for V_{SS} and V_5

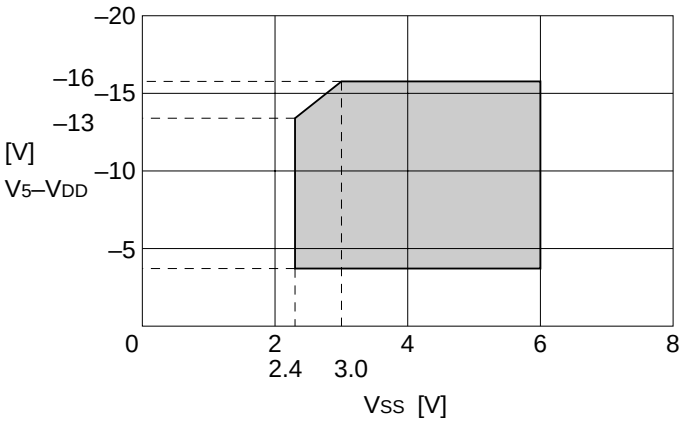


Figure 11

Power consumption during access (I_{DD} (2)) - MPU access cycle

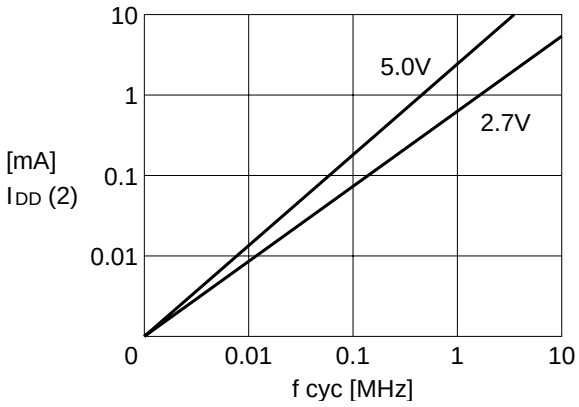


Figure 12

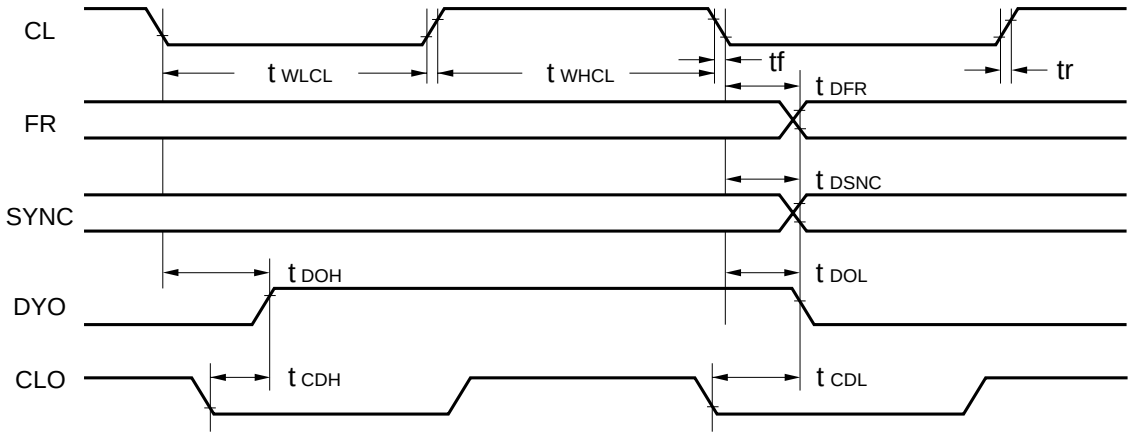
This graphic shows the current consumption when the vertical patterns are written during "fcyc". If not accessed, I_{DD}(1) is only shown.

Reset

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Reset time	t_R	See note.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

Note
t_R is measured from the rising edge of $\overline{RES}$. The SED1560 enters normal operating mode after a reset.

Display control timing



Input timing

V_{SS} = –5.5 to –4.5 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	30	—	ns
CL fall time	tf		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

V_{SS} = –4.5 to –2.7 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	40	—	ns
CL fall time	tf		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Notes: 1. Effective only when the SED156*DOB is in the master mode.
2. The FR/SYNC delay time input timing is provided in the slave operation.
The FR/SYNC delay time output timing is provided in the master operation.
3. Each timing is based on 20% and 80% of V_{SS}.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

Output timing

V_{SS} = –5.5 to –4.5 V, Ta = –30 to 85 deg. C

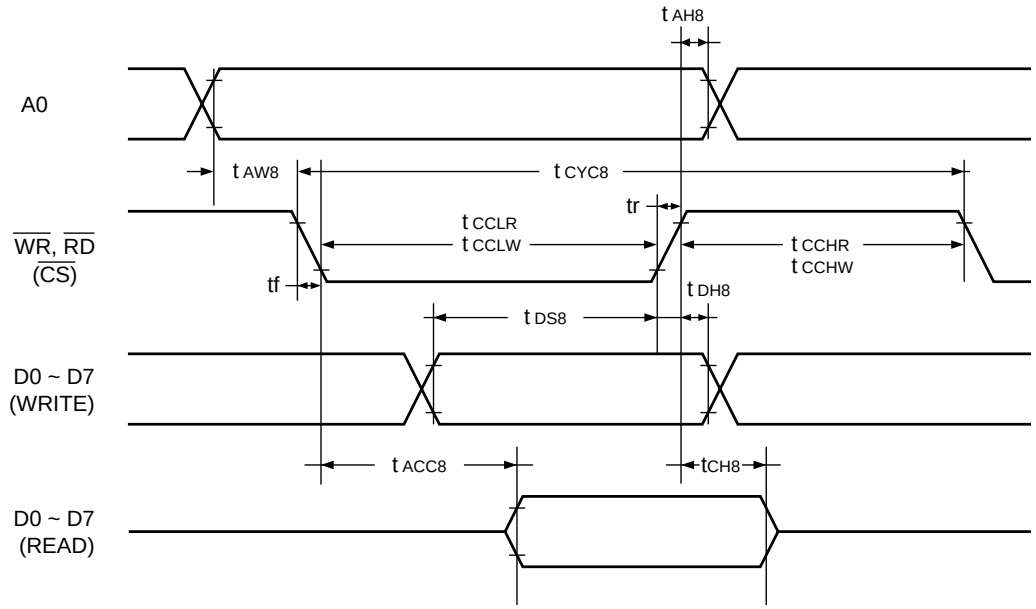
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	C_L = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}		—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO Low-level delay time	t_{CDL}	SED156✻D0B operating in master mode only	10	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156✻D0B operating in master mode only	10	40	100	ns

V_{SS} = –4.5 to –2.7 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	C_L = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}		—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156✻D0B operating in master mode only	10	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156✻D0B operating in master mode only	10	100	200	ns

(1) System buses

Read/write characteristics I (80-series MPU)



V_{SS} = –5.0 ±10%, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		10		ns
Address setup time		t_{AW8}		10		ns
System cycle time		t_{CYC8}		200		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22		ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77		ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172		ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f			15	ns

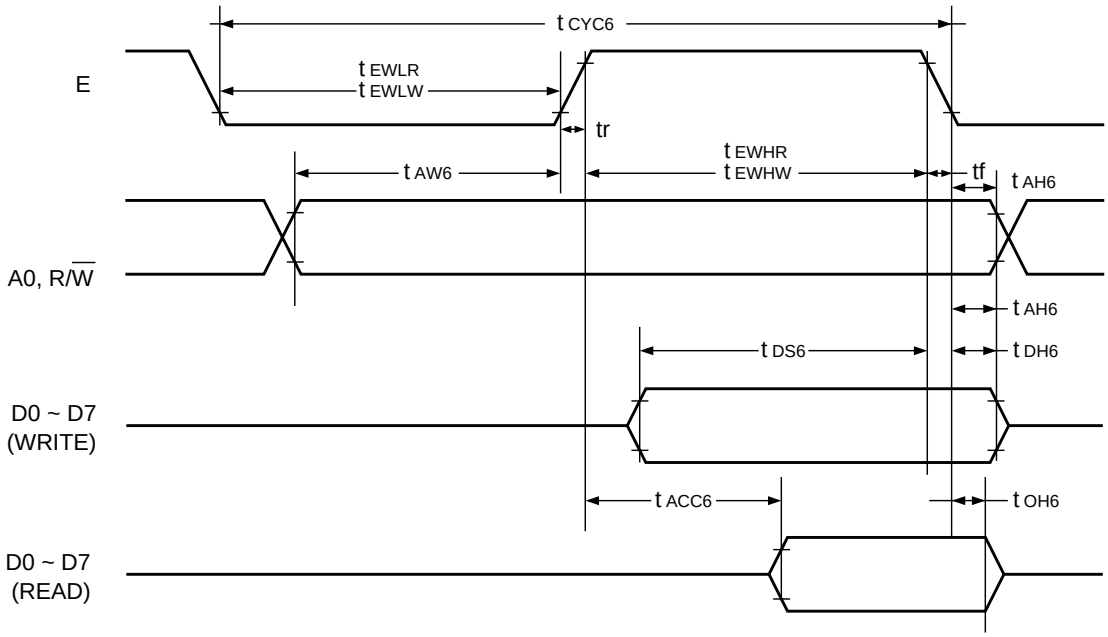
V_{SS} = –2.7 ~ –4.5 V, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		0		ns
Address setup time		t_{AW8}		0		ns
System cycle time		t_{CYC8}		450		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44		ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194		ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394		ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f			15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \le (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \le (t_{CYC8} - t_{CCLR} - t_{CCHR})$
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the RD or WR signal is in the low level.
   If read/write operation is performed by the RD or WR signal while CS is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.
   If read/write operation is performed by CS while the RD or WR signal is in the low level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(2) System buses

Read/write characteristics II (68-series MPU)



V_{SS} = –5.0 V ± 10%, Ta = –30 ~ 85 °C

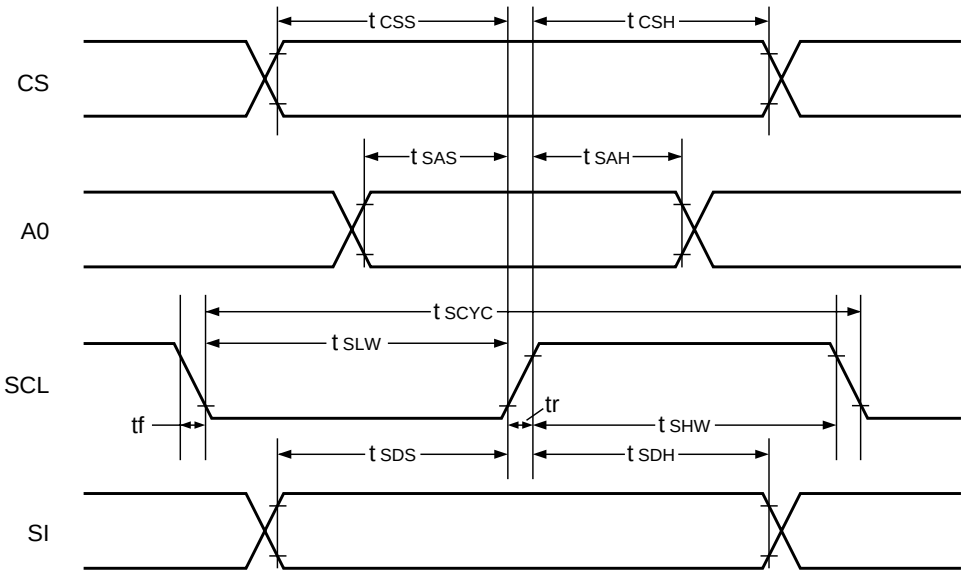
Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		200		ns
Address setup time		(A0)	t_{AW6}		10		ns
Address hold time		R/$\overline{W}$	t_{AH6}		10		ns
Data setup time		D0~D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		n
Output disable time			t_{OH6}	C_L = 100pF	10	50	ns
Access time			t_{ACC5}			70	ns
Enable H pulse width	READ	E	t_{EWHR}		77		ns
	WRITE		t_{EWHW}		22		ns
Enable L pulse width	READ	E	t_{EWLR}		117		ns
	WRITE		t_{EWLW}		172		ns
Input signal change time			t_r, t_f			15	ns

V_{SS} = –2.7 V ~ 4.5 V, Ta = –30 ~ 85 °C

Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		450		ns
Address setup time		A0	t_{AW6}		0		ns
Address hold time		R/$\overline{W}$	t_{AH6}		0		ns
Data setup time		D0 to D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		ns
Output disable time			t_{OH6}	C_L = 100pF	20	100	ns
Access time			t_{ACC5}			140	ns
Enable H pulse width	READ	E	t_{EWHR}		194		ns
	WRITE		t_{EWHW}		44		ns
Enable L pulse width	READ	E	t_{EWLR}		244		ns
	WRITE		t_{EWLW}		394		ns
Input signal change time			t_r, t_f			15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $t_r + t_f \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the E signal is in the high level. If read/write operation is performed by the E signal while CS is active, it is determined by the E signal timing.
   If read/write operation is performed by CS while the E signal is in the high level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(3) Serial interface



V_{SS} = –5.0 V ±10%, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250		ns
SCL High pulse width		t_{SHW}		75		ns
SCL Low pulse width		t_{SLW}		75		ns
Address setup time	A0	t_{SAS}		50		ns
Address hold time		t_{SAH}		200		ns
Data setup time	SI	t_{SDS}		50		ns
Data hold time		t_{SDH}		30		ns
CS-SCL time	CS	t_{CSS}		30		ns
		t_{CSH}		400		
Input signal change time		t_r, t_f			50	ns

V_{SS} = –2.7 V ~ –4.5 V, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500		ns
SCL High pulse width		t_{SHW}		150		ns
SCL Low pulse width		t_{SLW}		150		ns
Address setup time	A0	t_{SAS}		100		ns
Address hold time		t_{SAH}		400		ns
Data setup time	SI	t_{SDS}		100		ns
Data hold time		t_{SDH}		100		ns
CS-SCL time	CS	t_{CSS}		60		ns
		t_{CSH}		800		
Input signal change time		t_r, t_f			50	ns

*1. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
*2. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Parallel/serial interface

Parallel data can be transferred in either direction between the controlling microprocessor and the SED1560 series through the 8-bit I/O buffer (D0 to D7). Serial data can be sent from the microprocessor to the SED1560 series through the serial data input (SI), but not from the SED1560 series to the microprocessor. The parallel or serial interface is selected by P/S as shown in table 1.

Table 1. Parallel/serial interface selection

P/S	Input type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D0 to D7
HIGH	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	—	—	D0 to D7
LOW	Serial	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(Hz)

Note
"—" indicates fixed to either "H" or to "L"

For the parallel interface, the type of microprocessor is selected by C86 as shown in table 2.

Table 2. Microprocessor selection for parallel interface

C86	MPU bus type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	6800-series	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
LOW	8080-series	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Parallel interface

A0, $\overline{WR}$ (or R/W) and $\overline{RD}$ (or E) identify the type of parallel data transfer to be made as shown in table 3.

Serial interface

The serial interface comprises an 8-bit shift register and a 3-bit counter. These are reset when $\overline{CS1}$ is HIGH and CS2 is LOW. When these states are reversed, serial data and clock pulses can be received from the microprocessor on SI and SCL, respectively.

Table 3. Parallel data transfer

Common	6800 series		8080 series		Description
A0	R/W	E	$\overline{RD}$	$\overline{WR}$	
1	1	1	0	1	Display data read out
1	0	1	1	0	Display data write
0	1	1	0	1	Status read
0	0	1	1	0	Write to internal reigister (command)

Serial data is read on the rising edge of SCL and must be input at SI in the sequence D7 to D0. On every eighth clock pulse, the data is transferred from the shift register and processed as 8-bit parallel data.
Input data is display data when A0 is HIGH and control data when A0 is LOW. A0 is read on the rising edge of every eighth clock signal.
The SLC signal is affected by the termination reflection and external noise caused by the line length. The operation check on the actual machine is recommended.

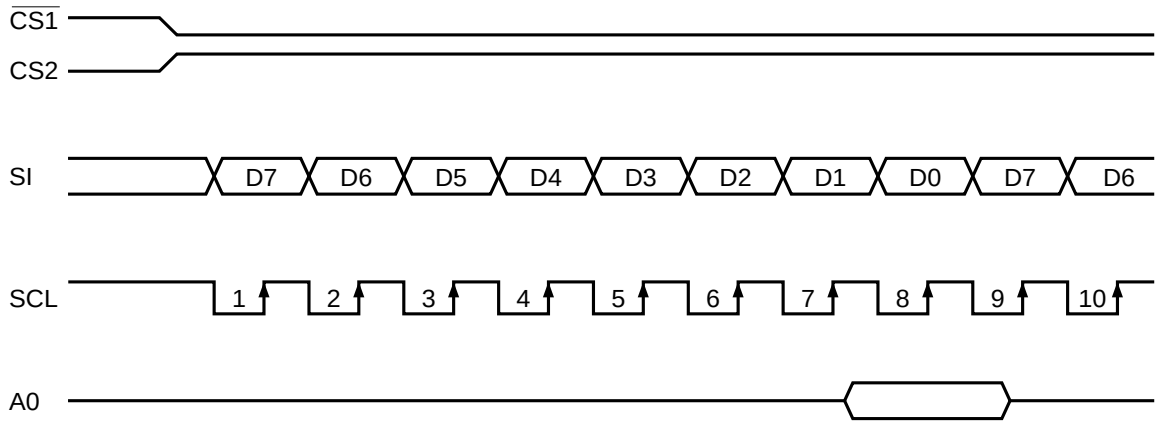


Figure 1. Serial interface timing

Chip select inputs

The SED1560 series has two chip select pins: $\overline{CS1}$ and CS2, and data exchange between the microprocessor and the SED1560 series is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH. When these pins are set to any other combination, D0 to D7 are high impedance. The A0, $\overline{RD}$, $\overline{WR}$, SI and SCI inputs are disabled. If the serial input interface has been selected, the shift register and counter are reset. The Reset signal is entered independent from the $\overline{CS1}$ and CS2 status.

Data Transfer

To match the timing of the display data RAM and registers to that of the controlling microprocessor, the SED1560 series uses an internal data bus and bus buffer. A kind of pipeline processing takes place. When the microprocessor reads the contents of RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Likewise, when the microprocessor writes data to display data RAM, the data is first stored in the bus buffer before being written to RAM at the next write cycle.

When writing data from the microprocessor to RAM, there is no delay since data is automatically transferred from the bus buffer to the display data RAM. If the data rate is required to slow down, the microprocessor can insert an NOP instruction which has the same affect as executing a wait procedure.

When a sequence of address sets is executed, a dummy read cycle must be inserted between each pair of address sets. This is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer, before it is sent to the microprocessor. A dummy read cycle is thus necessary after an address set and after a write cycle.

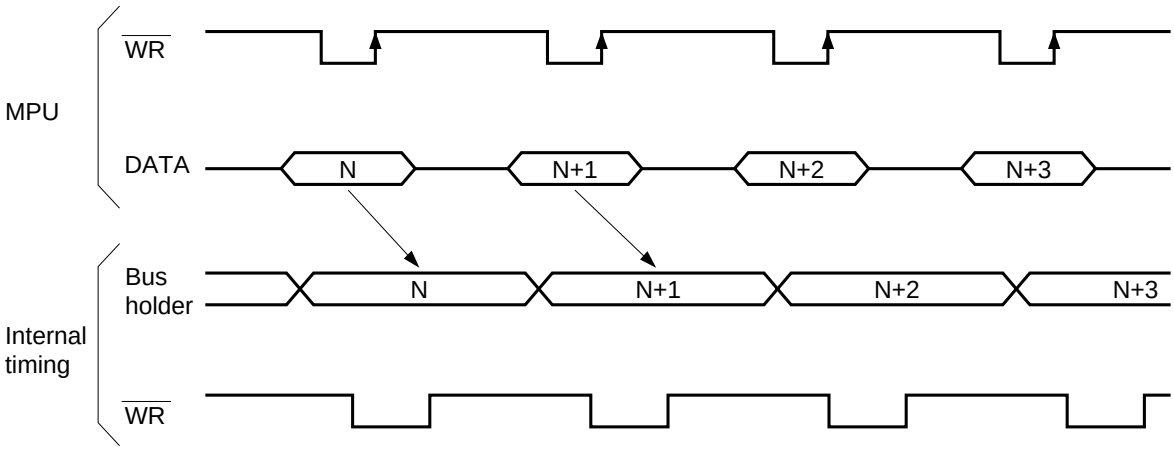


Figure 2. Write timing

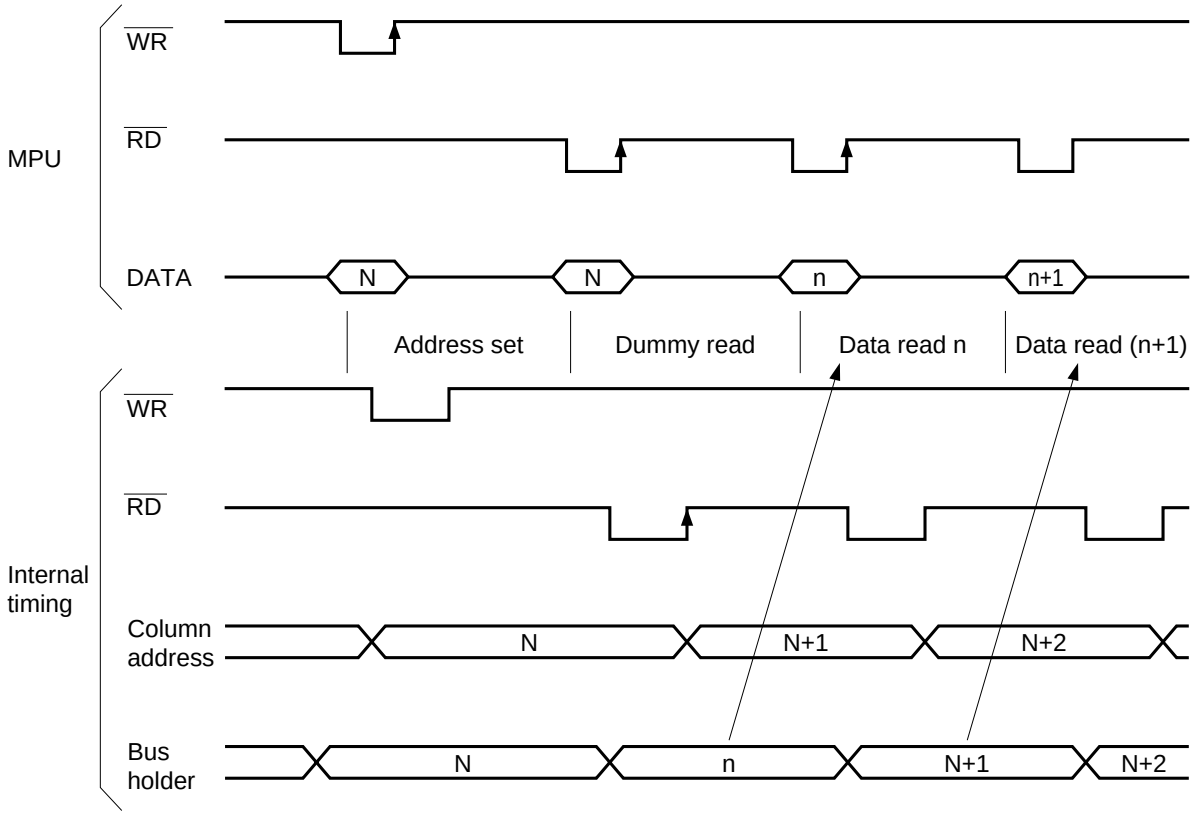


Figure 3. Read timing

Status Flag

The SED1560 series has a single bit status flag, D7. When D7 is HIGH, the device is busy and will only accept a Status Read command. If cycle times are monitored ed carefully, this flag does not have to be checked before each command, and microprocessor capabilities can be fully utilized.

Display Data RAM

The display data RAM stores pixel data for the LCD. It is a 166-column × 65-row addressable array as shown in figure 4.

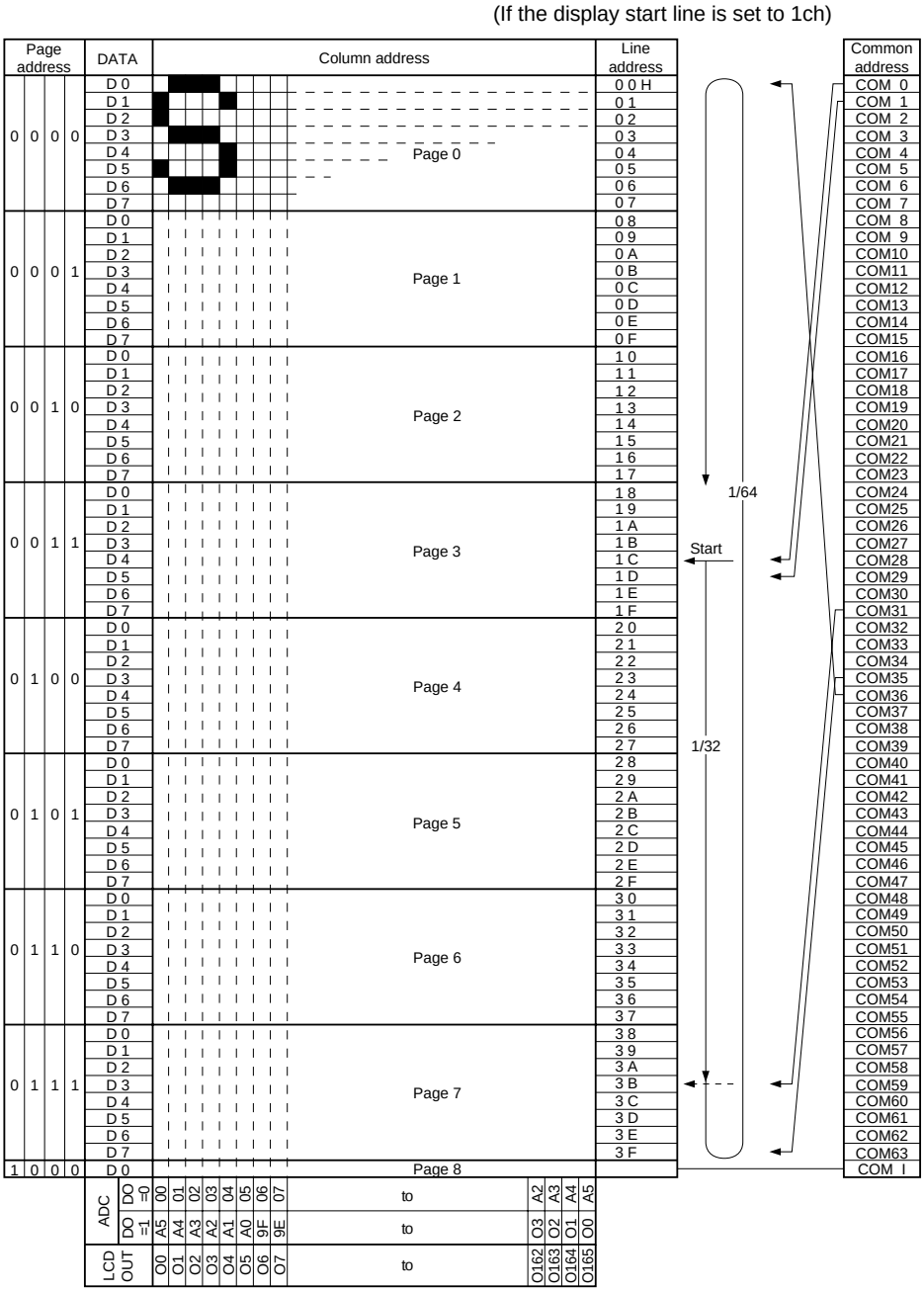


Figure 4. Display data RAM addressing

Note

For a 1/65 and 1/33 display duty cycles, page 8 is accessed following 1BH and 3BH, respectively.

The 65 rows are divided into 8 pages of 8 lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7.

The time taken to transfer data is very short, because the microprocessor inputs D0 to D7 correspond to the LCD common lines as shown in figure 5. Large display configurations can thus be created using multiple SED1560s.

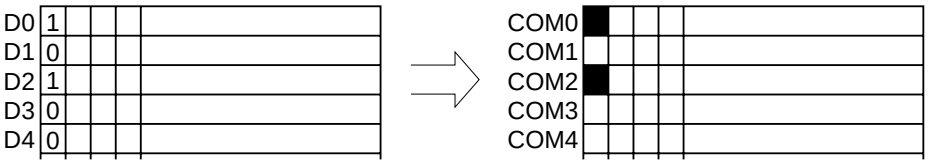


Figure 5. RAM-to-LCD data transfer

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flicker.

Column Address Counter

The column address counter is an 8-bit presettable counter that provides the column address to display data RAM. See figure 4. It is incremented by 1 each time a read or write command is received. The counter automatically stops at the highest address, A6H. The contents of the column address counter are changed by the Column Address Set command. This counter is independent of the page address register.
When the Select ADC command is used to select inverse display operation, the column address decoder inverts the relationship between the RAM column data and the display segment outputs.

Page Address Register

The 4-bit page address register provides the page address to display data RAM. The contents of the register are changed by the Page Address Set command.
Page address 8 (D3 = H, D2, D1, D0 = L) is a special use RAM area for the indicator.

Initial Display Line Register

The initial display line register stores the address of the RAM line that corresponds to the first (normally the top) line (COM0) of the display. See figure 4. The contents of this 6-bit register are changed by the Initial Display Line command. At the start of each LCD frame, synchronized with SYNC, the initial line is copied to the line counter. The line counter is then incremented on the CL clock signal once for every display line. This generates the line addresses for the transfer of the 166 bits of RAM data to the LCD drivers.
If a 1/65 or 1/33 display duty cycle is selected by the Duty + 1 command, the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected. If the Duty + 1 command is not used, the indicator special-use line address is not selected.

Output Selection Circuit

The number of common (COM) and segment (SEG) driver outputs can be selected to fit different LCD panel configurations by the output selection circuit.
There are 70 segment-only outputs (O32 to O101) and 96 common or segment dual outputs (O0 to O31 and O102 to O165). A command select the status of the dual common/segment outputs. Figure 6 shows the six different LCD driver arrangements.
Necessary LCD driver voltage is automatically allocated to the COM/SEG dual outputs when their function is determined by the output selection circuit.
The SED1560 selects Case 1, 2 or 6 while the SED1561 selects Case 3, 4, 5 or 6. As to the SED1562, COM/SEG output status cannot be selected, being fixed.

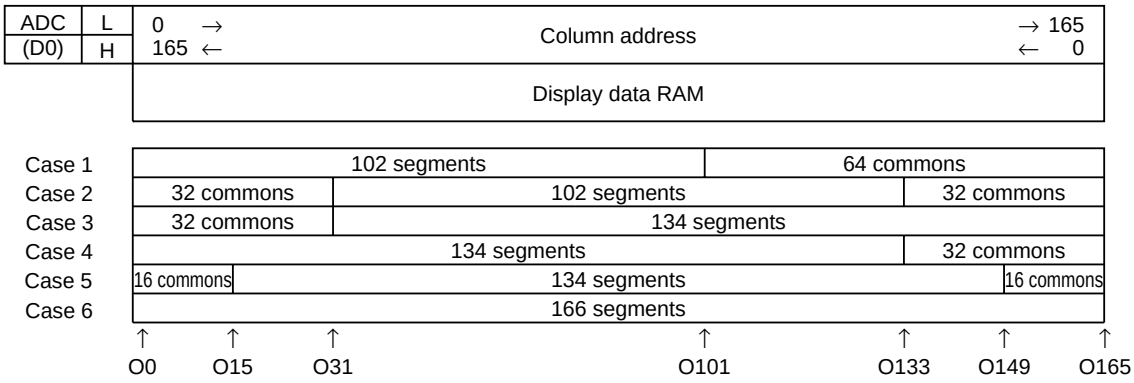


Figure 6. Output configuration selection

When COM outputs are assigned to the output drivers, the unused RAM area is not available. However, all RAM column addresses can still be accessed by the microprocessor.
Since duty setting and output selection are independent, the appropriate duty must be selected for each case.
Cases 1 to 6 are determined according to the three lowest bits in the output status register in the output selection circuit. The COM output scanning direction can be selected by setting bit D3 in the output status register to "H" or "L".

Table 4

	SED1560		SED1561		SED1562
Duty	1/64	1/48	1/32	1/24	1/16
COM I function	COM64	COM48	COM32	COM24	COM16

When the DUTY + 1 command is executed, pin COM1 becomes as shown in Figure 4 irrelevant to output selection:
Since master/slave operation and the output selection circuit are completely independent in the SED1560 series, a chip either on the master or slave side can be allocated to the COM output function in multi-chip configuration.
The LCD driver outputs shown in Table 5 become ineffective when the SED1560 or SED1561 is used with 1/48 or 1/24 duty, respectively. In this case, ineffective outputs are used in the open state.

Table 5

		Output status register				Ineffective output
		D3	D2	D1	D0	
SED1560	Case 1	0	1	0	1	O150 to O165
		1	1	0	1	O102 to O117
	Case 2	0	1	0	0	O150 to O165
		1	1	0	0	O16 to O31
SED1561	Case 3	0	0	1	1	O0 to O7
		1	0	1	1	O23 to O31
	Case 4	0	0	1	0	O158 to O165
		1	0	1	0	O134 to O141
	Case 5	0	0	0	1	O158 to O165
		1	0	0	1	O8 to O15

SED1560 Output Status

The SED1560 selects any output status from Cases 1, 2 and 6.

1/64 duty (Display Area 64 × 102)

Case	Status register				LCD driver output								
	D3	D2	D1	D0	O0		O31	O32		O101	O102	O133	O134		O165
1	0	1	0	1	SEG102						COM0 →				COM63
	1	1	0	1	SEG102						COM63 ←				COM0
2	0	1	0	0	COM31 ←		COM0	SEG102					COM32 →		COM63
	1	1	0	0	COM32 →		COM63	SEG102					COM31 ←		COM0
6	–	0	0	0	SEG166										

1/48 duty (Display Area 48 × 102)

Case	Status register				LCD driver output								
	D3	D2	D1	D0	O0		O31	O32		O101	O102	O133	O134		O165
1	0	1	0	1							COM0 →			COM47	
	1	1	0	1								COM47 ←			COM0
2	0	1	0	0	COM31 ←		COM0	SEG102					COM32→47		
	1	1	0	0	COM32→47			SEG102					COM31 ←		COM0
6	–	0	0	0	SEG166										

SED1561 Output Status

The SED1561 selects any output status from Cases 3, 4, 5 and 6.

1/32 duty (Display Area 32 × 134)

Case	Status register				LCD driver output										
	D3	D2	D1	D0	O0	O15	O16	O31	O32		O133	O134	149	150	O165
3	0	0	1	1	COM31 ←		COM0	SEG134							
	1	0	1	1	COM0 →		COM31	SEG134							
4	0	0	1	0	SEG134							COM0 →			COM31
	1	0	1	0	SEG134							COM31 ←			COM0
5	0	0	0	1	15←COM0		SEG134								COM16→31
	1	0	0	1	COM16→31		SEG134								15←COM0
6	–	0	0	0	SEG166										

1/24 duty (Display Area 24 × 134)

Case	Status register				LCD driver output										
	D3	D2	D1	D0	O0	O15	O16	O31	O32		O133	O134	149	150	O165
3	0	0	1	1		COM23 ←		COM0	SEG134						
	1	0	1	1	COM0 →		COM23		SEG134						
4	0	0	1	0	SEG134							COM0 →			COM23
	1	0	1	0	SEG134								COM23 ←		COM0
5	0	0	0	1	15←COM0		SEG134								16→23
	1	0	0	1	16→23		SEG134								15←COM0
6	–	0	0	0	SEG166										

SED1562 Output Status

COM/SEG output status of the SED1562 is fixed.
1/16 duty (16 × 150)

LCD driver output			
00	0149	150	0165
SEG150		15 ◄—	COM0

Display Timers

Line counter and display data latch timing

The display clock, CL, provides the timing signals for the line counter and the display data latch. The RAM line address is generated synchronously using the display clock. The display data latch synchronizes the 166-bit display data with the display clock.
The timing of the LCD panel driver outputs is independent of the timing of the input data from the microprocessor.

FR and SYNC

The LCD AC signal, FR, and the synchronization signal, SYNC, are generated from the display clock. The FR controller generates the timing for the LCD panel driver outputs. Normally, 2-frame wave patterns are generated, but *n*-line inverse wave patterns can also be generated. These produce a high-quality display if *n* is based on the LCD panel being used.
SYNC synchronizes the timing of the line counter and common timers. It is also needed to synchronize the frame period and a 50% duty clock.

In a multiple-chip configuration, FR and SYNC are inputs. The SYNC signal from the master synchronizes the line counter and common timing of the slave.

Common timing signals

The internal common timing and the special-use common driver start signal, DYO, are generated from CL. As shown in figures 7 and 8, DYO outputs a HIGH-level pulse on the rising edge of the CL clock pulse that precedes a change on SYNC. DYO is generated by both the SED1560D0B, regardless of whether the device is in master or slave mode. However, when operating in slave mode, the device duty and the external SYNC signal must be the same as that of the master. In a multiple-chip configuration, FR and SYNC must be supplied to the slave from the master.

Table 6. Master and slave timing signal status

Part number	Mode	FR	SYNC	CLO	DYO
SD156✻D✻B	Master	Output	Output	CL output	Output
	Slave	Input	Input	High impedance	Output

2-frame AC driver waveform

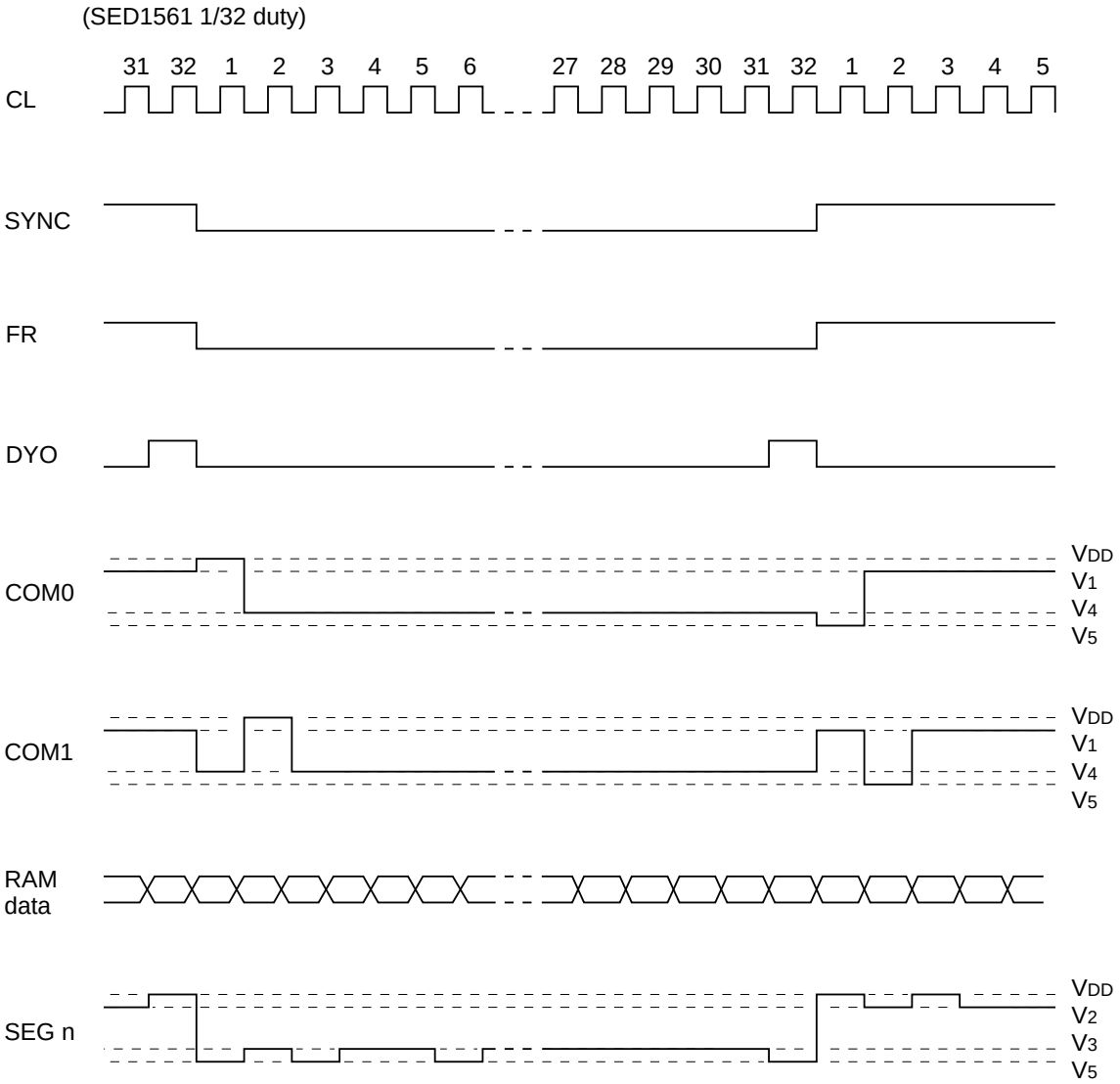


Figure 7. Frame driver timing

n line inverse driver waveform (n = 5, line inverse register 4)

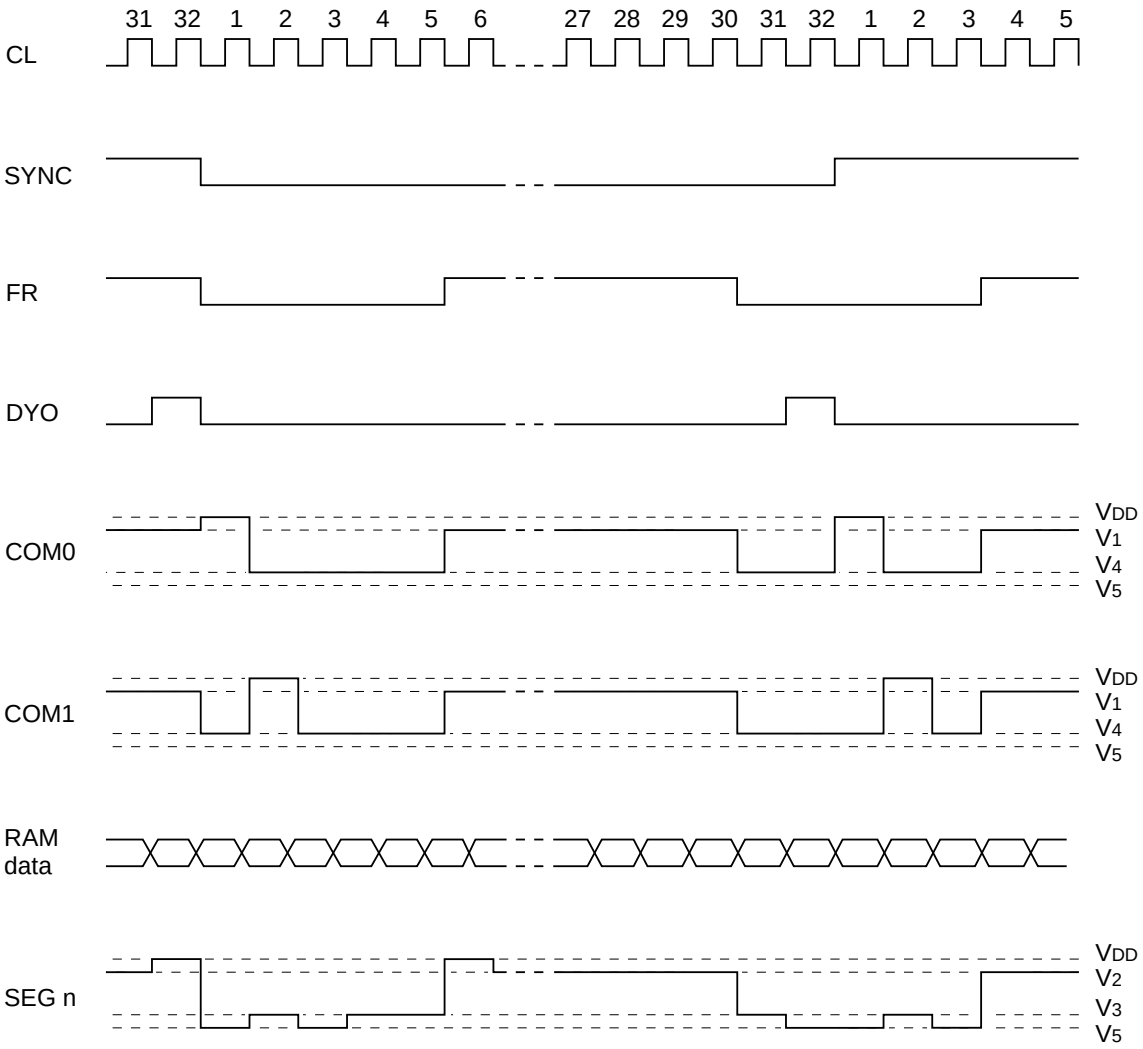


Figure 8. Line inverse driver timing

Note
When *n* = 5, the line inversion register is set to 4.

LCD Driver

The LCD driver converts RAM data into the 167 outputs that drive the LCD panel. There are 70 segment outputs, 96 segment or common dual outputs, and a COM1 output for the indicator display.

Two shift registers for the common/segment drivers are used to ensure that the common outputs are output in the correct sequence. The driver output voltages depend on the display data, the common scanning signal and FR.

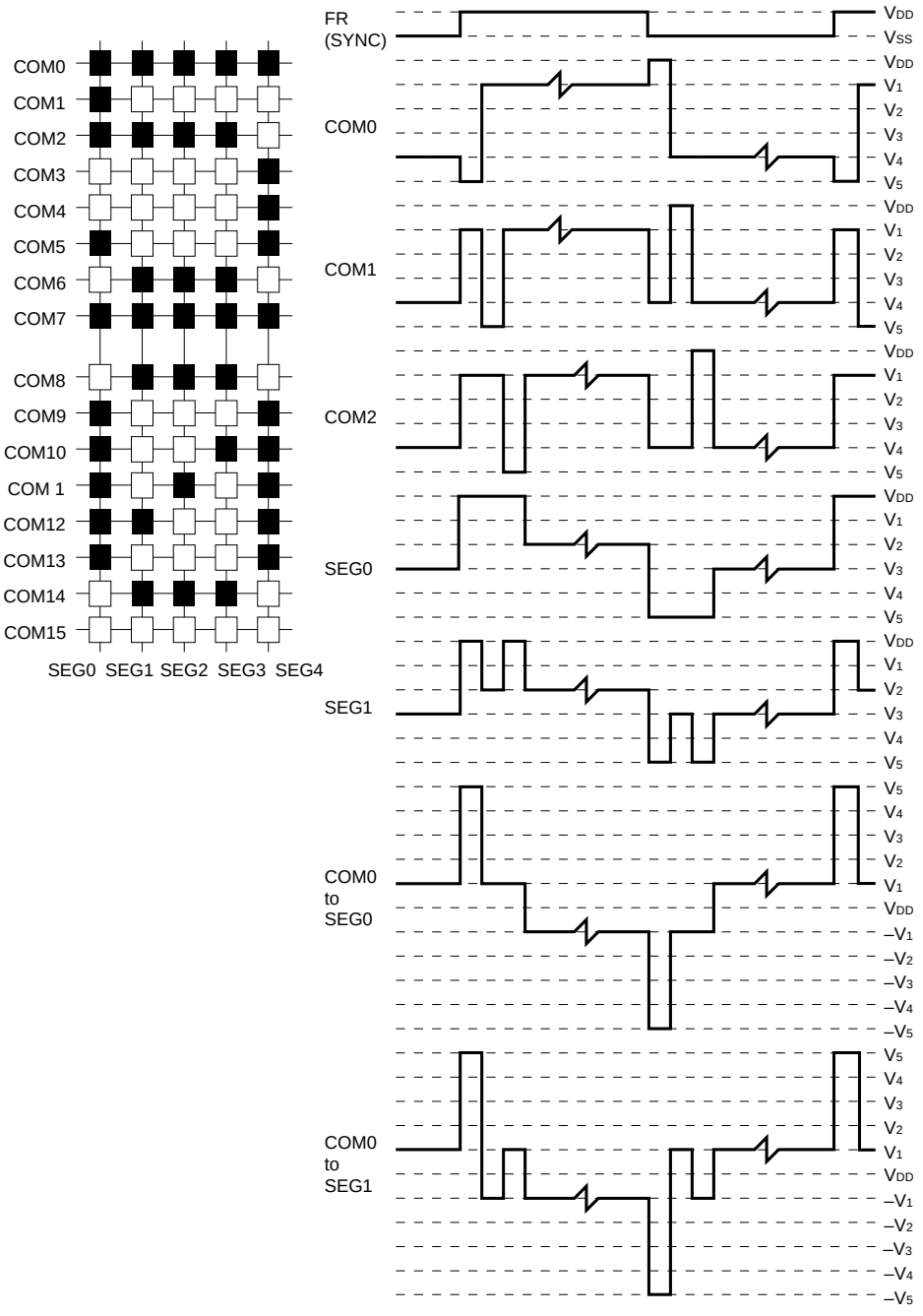


Figure 9. Example of segment and common timing

Display Data Latch Circuit

The display data latch circuit temporarily stores the output display data from the display data RAM to the LCD driver circuit in each common period. Since the Normal/Inverse Display, Display ON/OFF and Display All Points ON/OFF commands control the data in this latch, the data in the display data RAM is remains unchanged.

LCD Driver Circuit

This multiplexer generates 4-value levels for the LCD driver, having 167 outputs of 70 SEG outputs, 96 SEG/COM dual outputs and a COM output for the indicator display. The SEG/COM dual outputs have a shift register and sequentially transmits COM scanning signals. The LCD driver voltage is output according to the combination of display data, COM scanning signal and FR signal. Figure 9 shows a typical SEG/COM output waveform.

Oscillator Circuit

The low power consumption type CR oscillator adjusting the oscillator frequency by use of only oscillator resistor Rf is used as a display timing signal source or clock for the voltage raising circuit of the LCD power supply.
The oscillator circuit is only available in the master operation mode. When a signal from the oscillator circuit is used for display clock, fix the CL pin to the V_{SS} level. When the oscillator circuit is not used, fix the OSC1 or OSC2 pin to the V_{DD} or V_{SS} level, respectively.
The oscillator signal frequency is divided and output from the CLO pin as display clock. The frequency is divided to one-fourth, one-eighth or one-sixteenth in the SED1560, SED1561 or SED1562, respectively.

FR Control Circuit

The LCD driver voltage supplied to the LCD driver outputs is selected using FR signal.

Power Supply Circuit

This is a power circuit to produce voltage needed to drive liquid crystals at a low power consumption. This circuit is valid only when the SED156*D*B master is in operation. The power circuit consists of voltage tripler, voltage regulator and the voltage follower.
The power circuit built into SED1560*D*B is set for smaller scale liquid crystal panels and it is not too suitable when the picture element is larger or to drive a liquid crystal panel with lager indication capacity using multiple chips. With liquid crystal panels with a larger load capacity, the quality of display may become very bad. Use an external power in such cases. (If an external amp circuit is configured, we recommend to use the SCI7660 and SCI7661.)
The power circuit can be controlled by the built-in power ON/OFF command. When the built-in power is turned off, all of the boosting circuit, voltage regulation circuit and voltage follower circuit goes open. In this case, the liquid crystal driving voltage V_1, V_2, V_3, V_4 and V_5 should be supplied from outside and the terminals CAP1+, CAP1-, CAP2+, CAP2-, Vout and V_R should be kept opened.
If the built-in power supply is turned on, you must always enter this command after the wait time of the built-in power supply turn-on completion command.
Various functions of the power circuit may be selected by combinations of the setting of the T1 and T2. It is also possible to make a combined use of the external power supply and a portion of the functions of the built-in power supply.

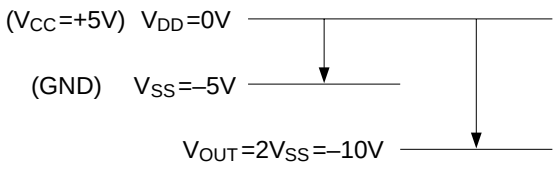
T1	T2	Voltage tripler	Voltage regulator	voltage follower	External voltage input	Voltage tripler terminals	V_R terminals
L	L	○	○	○	–		
L	H	○	○	○	–		
H	L	×	○	○	V_{OUT}	OPEN	
H	H	×	×	○	V_5	OPEN	OPEN

When (T1, T2) = (H, L), the boosting circuit does not work and open the boosting circuit terminals (CAP1+, CAP1-, CAP2+ and CAP2-) and apply liquid crystal driving voltage to the Vout terminals from outside.

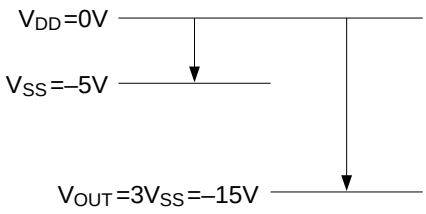
When (T1, T2) = (H. H), the boosting circuit and voltage regulation circuit do not work and open the boosting circuit terminals and the VR terminals and apply liquid crystal driving voltage connecting the V_5 terminals.

Voltage tripler

By connecting capacitors C1 between CAP1+ and CAP1-, CAP2+ and CAP2- and VSS-Vout, the electric potential between VDD-VSS is boosted to the triple toward negative side and outputted from the Vout terminal. When a double boosting is required, disconnect the capacitor between CAP2+ and CAP2- and short-circuit the CAP2- and Vout terminals to obtain output boosted to the double out of the Vout (or CAP2-) terminal.
Signals from the oscillation circuit are used in the boosting circuit and it then is necessary that the oscillation circuit is in operation.
Electric potentials by the boosting functions are given below.



Electric potentials of double boosting



Electric potentials of triple boosting

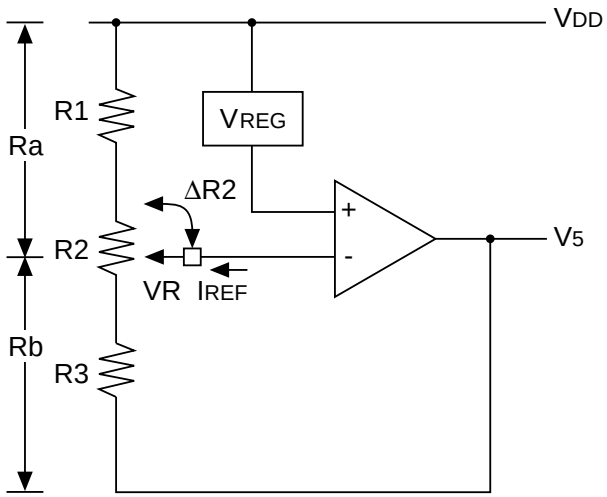
Voltage Regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator, and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V_5| < |V_{OUT}|$.

$$V_5=(1+\frac{Rb}{Ra})\ V_{REG}+I_{REF}\cdot Rb$$

$$=(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2})\ V_{REG}$$

$$+I_{REF}\cdot(R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and it is constant and $V_{REG} \fallingdotseq -2.5 \pm 0.15$ V (if V_{DD} is 0 V). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3: (In case of Type 1)

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots\cdots\cdots \textcircled{1}$$

(As I_{REF} = 0 A)

- R1 + R2 + R3 = 5MΩ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 V_5 = –6 to –10 V
  (Determined by the LCD characteristics)
  ΔR2 = OΩ, V_{REG} = –2.55V
  To obtain V_5 = -10 V, from equation ①:
  R2 + R3 = 2.92 × R1 ..... ③
  ΔR2 = R2, V_{REG} = –2.55V
  To obtain V_5 = -6 V, from equation ①:
  1.35 × (R1 + R2) = R3 ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
In case of Type 2, similarly preset R1, R2 and R3 on the basis of $V_{REG} = V_{SS}$.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage. This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra}) V_{REG} + Rb \times \Delta I_{REF} \quad \text{..... ⑤}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below.
Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.5V±0.15V } Type1
V_{REG} = –0.2%/˚C
V_{REG} = V_{SS} }Type2
V_{REG} = 0.00%/˚C
V_{REG} = –0.2%/°C
I_{REF} = –3.2µA±40% (For 16 levels)
I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)
0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

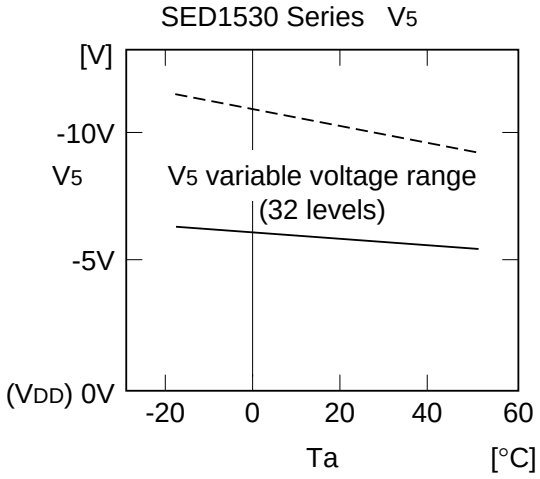
$$R3 = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{4V}{6.5\mu A}$$

$$\underline{Rb = 625K\Omega}$$

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5 max}{V_{REG}} - 1} = \frac{625K\Omega}{\frac{-6V}{-2.55V} - 1}$$

$$\underline{Ra = 462K\Omega}$$



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (-2.55V)$
$= -6.0V$
$V_5min = V_5\ max + Rb \times I_{REF}$
$= -6V + 625k \times (-6.5\mu A)$
$= -10.0V$

Ta=–10°C

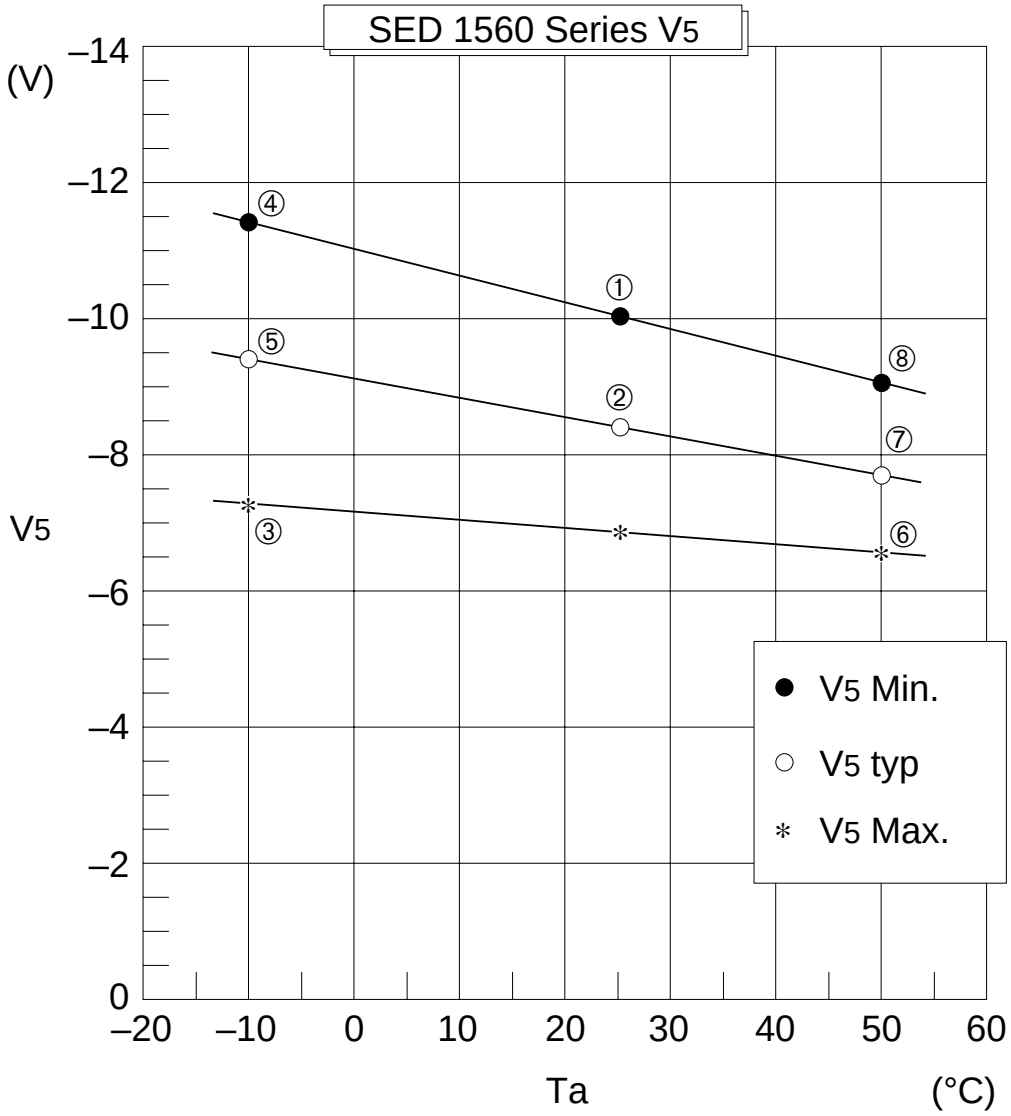
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (-2.55V) \times \{1+(-0.2\%/°C) \times (-10°C-25°C)\}$
$= -6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= -6.42V + 625k \times \{-6.5\mu A+(0.052\mu A/°C) \times (-10°C-25°C)\}$
$= -11.63V$

Ta=–50°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (-2.55V) \times \{1+(-0.2\%/°C) \times (50°C-25°C)\}$
$= -5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= -5.7V + 625k \times \{-6.5\mu A+(0.052\mu A/°C) \times (50°C-25°C)\}$
$= -8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.
In case of Type 2, it so becomes that $V_{REG} = V_{SS}$ (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

Example of V_5 Voltage When Using SED1560 Series Electronic Volume



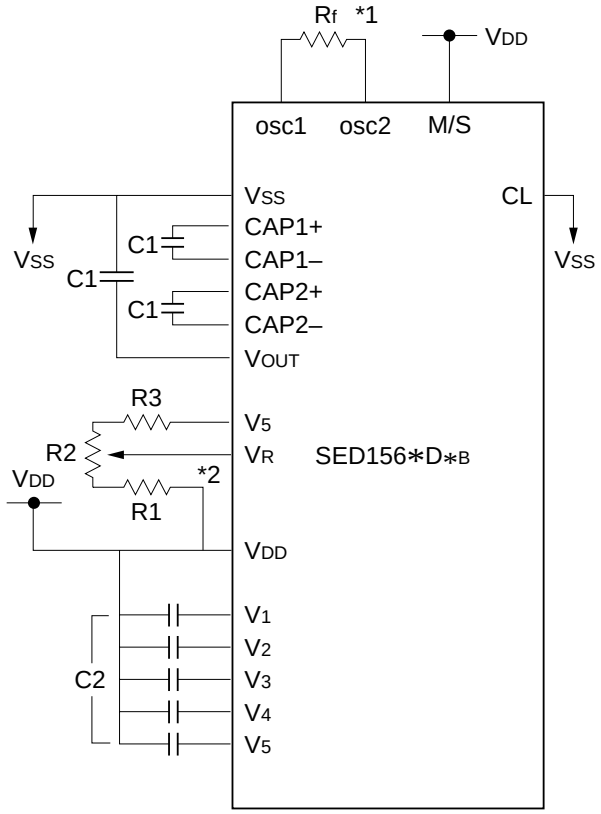
Liquid Crystal Voltage Generating Circuit

A V_5 potential is resistively divided within the IC to cause V_1, V_2, V_3 and V_4 potentials needed for driving of liquid crystals. The V_1, V_2, V_3 and V_4 potentials are further converted in the impedance by the voltage follower before supplied to the liquid crystal driving circuit. The liquid crystal driving voltage is fixed with each type.

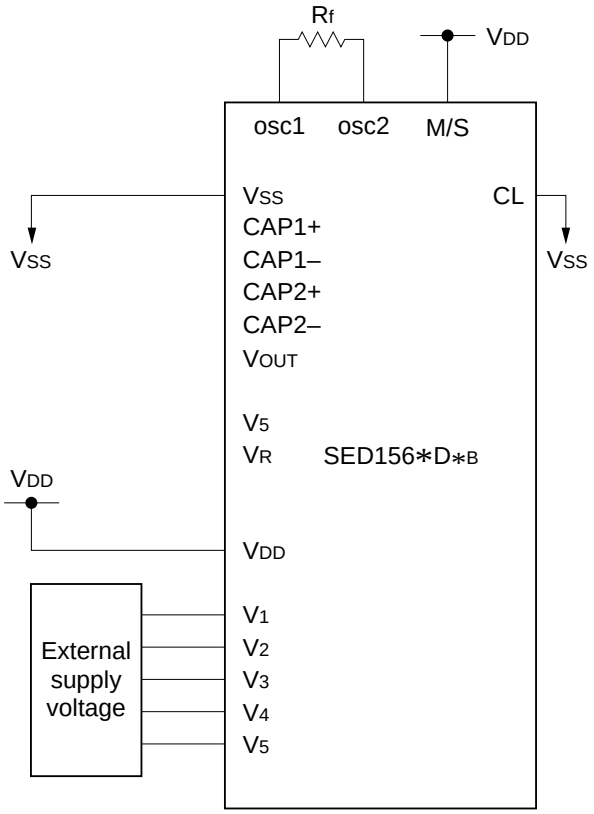
types	Liquid crystal driving voltage
SED1560D0B	1/9 bias voltage
SED1560DAB	1/7 bias voltage
SED1561D0B	1/7 bias voltage
SED1561DAB	1/5 bias voltage
SED1562D0B	1/5 bias voltage

As shown in Fig. 8, it needs to connect, externally voltage stabilizing capacitors C2 to the liquid crystal power terminals. When selecting such capacitor C2 make actual liquid crystal displays matching to the display capacity of the liquid crystal display panel, before determining on the capacitance as the constant value for voltage stabilization.

When the built-in power circuit is used



When the built-in power circuit is not used



Reference set values:

SED1560 V_5 ≒ –11~ –13 V
SED1561 V_5 ≒ –7~ –9 V
SED1562 V_5 ≒ –5~ –7 V (Variable)

	SED1560	SED1561	SED1562
C1	4.7 µF	2.2 to 4.7 µF	2.2 to 4.7 µF
C2	0.1 to 0.47 µF	0.1 to 0.47 µF	0.1 µF
R1	1 MΩ	700 KΩ	500 KΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	4 MΩ	1.6 MΩ	700 KΩ
LCD SIZE	32×51 mm	16×67 mm	8×75 mm
DOT	64×102	32×134	16×150

*1 Connect oscillator feedback resistor Rf as short as possible and place it close to the IC for preventing a malfunction.

*2 Use short wiring or shielded cables for the VR pin due to high input impedance.

*3 Determine C1, C2 depending on the size of LCD panel driven. You must set these values so that the LCD driving voltage becomes stable. Set (T1, T2)=(H, L) and supply an external voltage to VOUT. Display the LCD heavy load pattern and determine C2 so that the LCD driving voltages (V_1 to V_5) become stable. Then, set (T1, T2)=(L, L) and determine C1.
Set the same capacitance for C2.

*4 The "LCD SIZE" indicates the vertical and horizontal length of the LCD panel display area.

* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

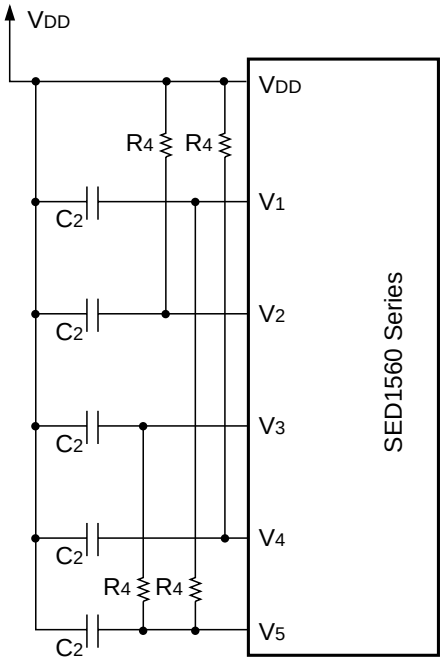
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

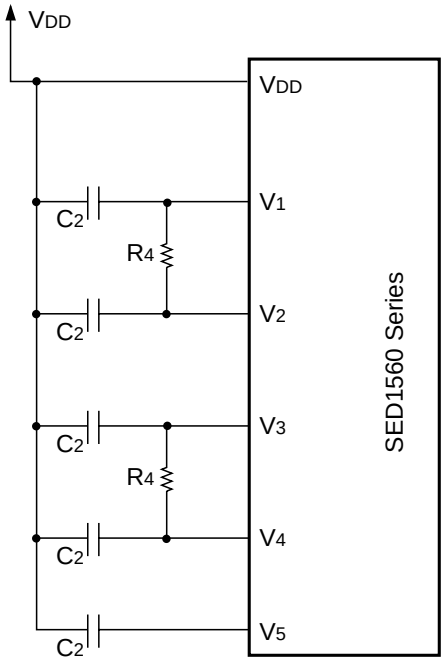
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reset

When power is turned ON, the SED1560 is initialized on the rising edge of $\overline{RES}$. Initial settings are as follows.

1. Display : OFF
2. Display mode : Normal
3. *n*-line inversion : OFF
4. Duty cycle : 1/64 (SED1560)
   1/32 (SED1561)
5. ADC select : Normal (D0 = L)
6. Read/write modify : OFF
7. Internal power supply : OFF
8. Serial interface register data : Cleared
9. Display initial line register : Line 1
10. Column address counter : 0
11. Page address register : Page 0
12. Output selection circuit : Case 6
13. *n*-line inversion register : 16
14. Set the electronic control register to zero (0).

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 µs to correctly reset the SED1560. Normal operation starts 1 µs after the rising edge on $\overline{RES}$.

If the built-in LCD power circuit of the SED156✻D✻B is not used, the $\overline{RES}$ signal must be low when the external LCD power supply is turned on. When the $\overline{RES}$ goes low, each register is cleared to the above listed initial status. However, the oscillation circuit and output pins (OSC2, FR, SYNC, CLD, DYO, D0 to D7 pins) are not affected.

If the SED1560 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

Although SED1560 Series devices maintain the operation status under commands, when external noise of excessive levels enters, their internal statys may be changed. Consequently, it is necessary to provide means to suppress noise occurring from package or the system or orovide means to avoid influence of such noise.

Also, to cope with sudden noise, we suggest you to set up the software so the operation status can be periodically refreshed.

When the Reset command is used, only initial settings 9 to 14 are active.

COMMANDS

The Command Set

A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed.

For the 80-series MPU interface, the command is activated when a low pulse is entered in the $\overline{RD}$ pin during read or when a low pulse is entered in the $\overline{WR}$ pin during write. While the 68-series MPU interface is set to the read status when a high pulse is entered in the R/$\overline{W}$ pin, and it is set to the write status when a low pulse is entered in this pin. The command is activated when a high pulse is entered in the E pin. (For their timings, see Section 10 "Timing Characteristics.") Therefore, the 68-series MPU interface differs from the 80-series MPU interface in the point where the $\overline{RD}$ (or E) signal is 1 (or high) during status read and during display data read explained in the command description and on the command table. The following command description uses an 80-series MPU interface example.

If the serial interface is selected, data is sequentially entered from D7.

Table 7. SED1560 series command table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LCD display ON and OFF 0 : OFF 1 : ON
Display START Line set	0	1	0	0	1	Dispaly start address						Determines the RAM display line for COM 0
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register.
Column address set; high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high-order 4 bits of the display RAM column address in the register.
Column address set; low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RAM column address in the register.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Status read	0	0	1	Status				0	0	0	0	Reads the status information.
Display data write	1	1	0	Write Data								Writes data in the display RAM.
Display data read	1	0	1	Read Data								Reads data from the display RAM.
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Outputs the display RAM address for SEG. 0: Normal 1: Reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Displays the LCD image in normal or reverse mode. 0: Normal 1: Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all indicators. 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0:1/24, 48 1:1/32, 64
Duty +1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0: Normal 1: Duty+1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the line reverse driving and No. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.
Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address counter, and set to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indictors.

Commands

Display ON/OFF

Alternatively turns the display ON and OFF.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	1	1	D

Note
D = 0 Display OFF
D = 1 Display ON

Initial Display Line

Loads the RAM line address of the initial display line, COM0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
↓						↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Page Address Set

Loads the RAM page address from the microprocessor into the page address register. A page address, along with a column address, defines a RAM location for writing or reading display data. When the page address is changed, the display status is not affected.
Page address 8 is a special use RAM area for the indicator. Only D0 is available for data exchange.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

Column Address Set

Loads the RAM column address from the microprocessor into the column address register. The column address is divided into two parts-4 high-order bits and 4 low-order bits.
When the microprocessor reads or writes display data to or from RAM, column addresses are automatically incremented, starting with the address stored in the column address register and ending with address 166. The page address is not incremented automatically.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	A7	A6	A5	A4

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
↓								↓
1	0	1	0	0	1	0	1	165

Read status

Indicates to the microprocessor the four SED1560 status conditions.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	Busy	ADC	ON/ OFF	RES- ET	0	0	0	0

BUSY — Indicates whether or not the SED1560 will accept a command. If BUSY is 1, the device is currently executing a command or is resetting, and no new commands can be accepted. If BUSY is 0, a new command can be accepted. It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed.

ADC — Indicates the relationship between RAM column addresses and the segment drivers. If ADC is 1, the relationship is normal and column address *n* corresponds to segment driver *n*. If ADC is 0, the relationship is inverted and column address (165 – *n*) corresponds to segment driver *n*.

ON/OFF — Indicates whether the display is ON or OFF. If ON/OFF is 1, the display is OFF. If ON/OFF is 0, the display is ON. Note that this is the opposite of the Display ON/OFF command.

RESET — Indicates when initialization is in process as the result of RES or the Reset command.

Write Display Data

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page.

A_0	$\overline{RD}$ E	$\overline{WR}$ R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Read Display Data

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continously read data from the addressed page. A dummy read is required after loading an address into the column address register.
Display data cannot be read through the serial interface.

A_0	$\overline{RD}$ E	$\overline{WR}$ R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Select ADC

Selects the relationship between the RAM column addresses and the segment drivers. When reading or writing display data, the column address is incremented as shown in figure 4.

A_0	$\overline{RD}$ E	$\overline{WR}$ R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

Note
D = 0 Rotate right (normal direction)
D = 1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor. There are very few restrictions on pin assignments when constructing an LCD module.

Normal/Inverse Display

Determines whether the data in RAM is displayed normally or inverted.

A_0	$\overline{RD}$ E	$\overline{WR}$ R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	1	D

Note
D = 0 LCD segment is ON when RAM data is 1 (normal).
D = 1 LCD segment is ON when RAM data is 0 (inverse).

Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM. The RAM contents are not changed. This command has priority over the normal/inverse display command.

A_0	$\overline{RD}$ E	$\overline{WR}$ R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	0	D

Note
D = 0 Normal display status
D = 1 All display segments ON

If this command is received when the display status is OFF, the Power Save command is executed.

Select Duty

Selects the LCD driver duty.
Since this is independent from contents of the output status register, the duty must be selected according to the LCD output status.
In multi-chip configuration, the master and slave devices must have the same duty.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
SED1560	0 1	1/48 1/64
SED1561	0 1	1/24 1/32
SED1562	0 1	1/16 1/16

Duty + 1

Increases the duty by 1. If 1/48 or 1/64 duty is selected in the SED1560 for example, 1/49 or 1/65 is set, respectively and COM1 functions as either the COM48 or COM64 output. The display line always accesses the RAM area corresponding to page address 8, D0. (Refer to Figure 4.)
In multi-chip configuration, the Duty + 1 command must be executed to both the master and slave sides.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
SED1560	0 1	1/48 or 1/64 1/49 or 1/65
SED1561	0 1	1/24 or 1/32 1/25 or 1/33
SED1562	0 1	1/16 1/17

Set *n*-lineE Inversion

Selects the number of inverse lines for the LCD AC controller. The value of *n* is set between 2 to 16 and is stored in the *n*-line inversion register.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of inverted lines
0	0	0	0	–
0	0	0	1	2
0	0	1	0	3
↓				↓
1	1	1	0	15
1	1	1	1	16

Do not use this command when using the votage follower of the built-in power supply, the characteristics of the built-in power supply cannot then be guaranteed to stay within the specification.

Cancel *n*-line Inversion

Cancels *n*-line inversion and restores the normal 2-frame AC control. The contents of the *n*-line inversion register are not changed.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0

Modify Read

Following this command, the column address is no longer incremented automatically by a Read Display Data command. The column address is still incremented by the Write Display Data command. This mode is cancelled by the End command. The column address is then returned to its value prior to the Modify Read command. This command makes it easy to manage the duplication of data from a particular display area for features such as cursor blinking.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note that the Column Address Set command cannot be used in modify-read mode.

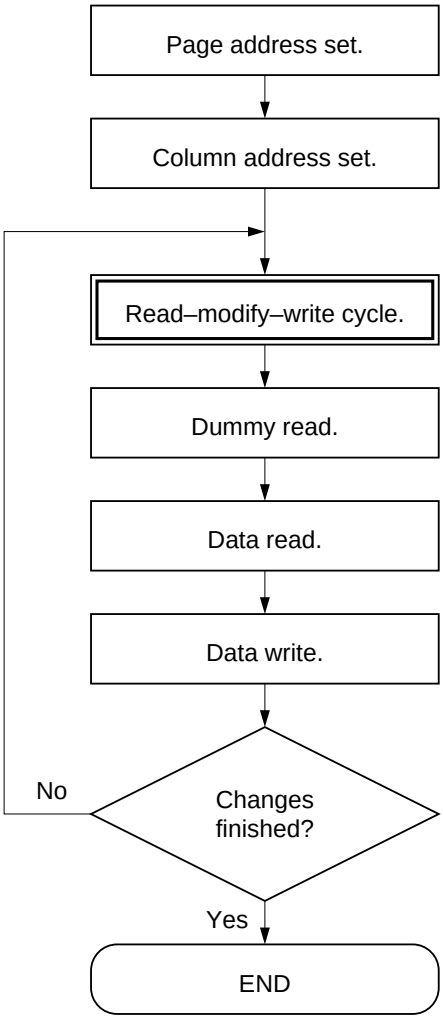


Figure 13. Command sequence for cursor blinking

End

Cancels the modify read mode. The column address prior to the Modify Read command is restored.

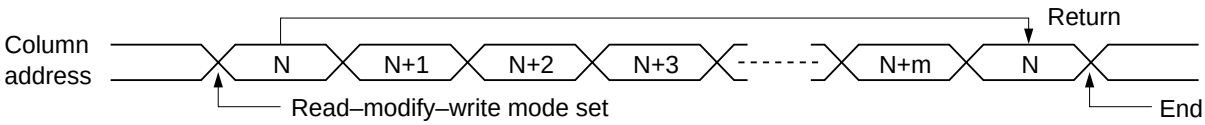
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

Resets the initial display line, column address, page address, and *n*-line inversion registers to their initial values. This command does not affect the display data in RAM.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply. Only RES can be used to initialize the supplies.



Output Status Register

Available only in the SED1560 and SED1561.
This command selects the role of the COM/SEG dual pins and determines the LCD driver output status.
The COM output scanning direction can be selected by setting A3 to "H" or "L". For details, refer to the Output Status Circuit in each function description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

A3: Selection of the COM output scanning direction

A_2 A_1 A_0	Output Status	Number of COM/SEG Output pins	Remarks
0 0 0	Case 6	SEG 166	Applies to the SED1560/61
0 0 1	Case 5	SEG 134, COM 32	Applies to the SED1561
0 1 0	Case 4	SEG 134, COM 32	
0 1 1	Case 3	SEG 134, COM 32	
1 0 0	Case 2	SEG 102, COM 64	Applies to the SED1560
1 0 1	Case 1	SEG 102, COM 64	
1 1 0	Case 6	SEG 166	Applies to the SED1560/61
1 1 1	Case 6	SEG 166	

LCD Power Supply ON/OFF

Turns the SED156*D*B internal LCD power supply ON or OFF. When the power supply is ON, the voltage converter, the voltage regulator circuit and the voltage followers are operating. For the converter to function, the oscillator must also be operating.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0

Note
D = 0 Supply OFF
D = 1 Supply ON

When an external power supply is used with the SED156*D*B, the internal supply must be OFF.
If the SED156*D*B is used in a multiple-chip configuration, an external power supply that meets the specifications of the LCD panel must be used. An SED1560 operating as a slave must have its internal power supply turned OFF.

Completion of Built-in Power On

This command turns on the built-in power supply.

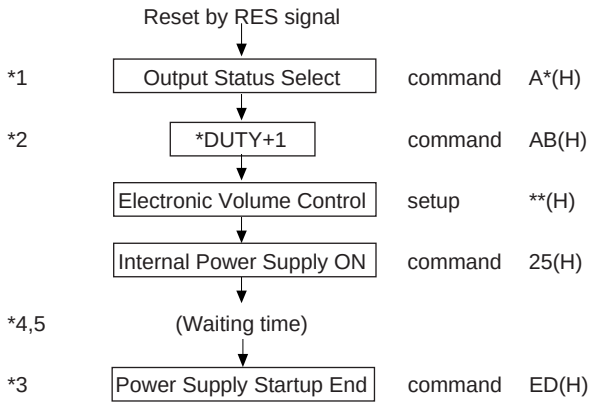
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

The SED1560 series has the built-in, low-power LCD driving voltage generator circuit which can cut almost all currents except those required for LCD display. This is the primary advantage of the SED1560 series product. However, it has the low power and you need perform the following power-on sequence when turning on the built-in power supply:

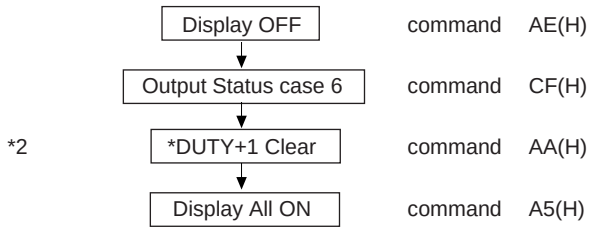
Sequence in the Built-in Power supply ON/OFF Status

To turn on built-in power supply, execute the above built-in power supply ON sequence. To turn off internal power supply execute the power save sequence as shown in the following power supply OFF status. Accordingly, to turn on built-in power supply again after turn it off (power save), execute the "Power Save Clear Sequence" that will be described afterwards.

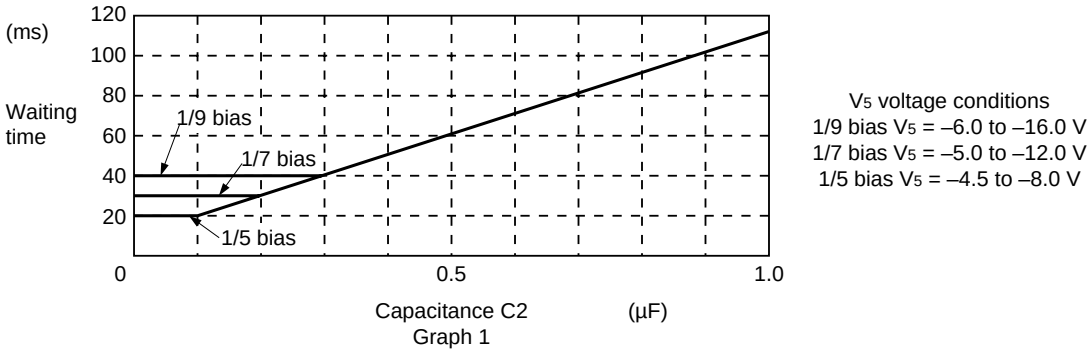
Built-in power supply ON status



Built-in power supply OFF status



*1: Regarding the SED 1562, it is not necessary to execute a command to decide an output status.
*2: When the COMI pin is not used, it is not necessary to enter the DUTY+1 and DUTY+1 Clear commands.
*3: When the built-in power supply startup end command is not executed, current is consumed stationarily.
Built-in power supply startup end command must always be used in a pair with built-in power supply ON command.
*4: The waiting time depends on the externally-installed capacitance C2 (refer to 4-35). After the waiting time shown in Graph 1, the power supply can be started surely.



Graph 1

*5: Within the waiting time in built-in power supply ON status, any command other than built-in power supply control commands such as Power Save, and display ON/OFF command, display normal rotation/reverse command, display all ON command, output status select command and DUTY+1 clear command can accept another command without any problem. RAM read and write operations can be freely performed.

Electronic Volume Control Register

Through these commands, the liquid crystal driving voltage V5 being outputted from the voltage regulation circuit of the built-in liquid crystal power supply, in order to adjust the contrast of the liquid crystal display.
By setting data to the 4 bit register, one of the 16 voltage status may be selected for the liquid crystal driving voltage V5. External resistors are used for setting the voltage regulation range of the V5. For details refer to the paragraph of the voltage regulation circuit in the Clause for the explanation of functions.

A0	$\overline{E}$ / RD	R/$\overline{W}$ / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	A5	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	| V5 |
0	0	0	0	0	Small (as the absolute value)
		:			
		:			
1	1	1	1	1	Large (as the absolute value)

When not using the electronic volume control function, set to (0, 0, 0, 0, 0).

Power Save (Complex Command)

If the Display All Points ON command is specified in the display OFF state, the system enters the power save status, reducing the power consumption to approximate the static power consumption value. The internal state in the power save status is as follows:

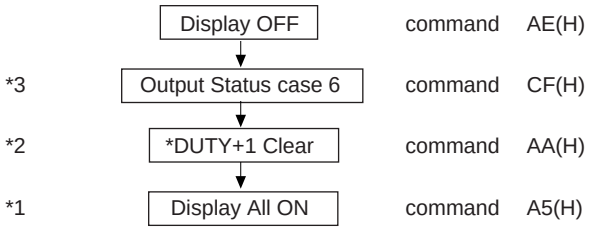
(a) The oscillator and power supply circuits are stopped.
(b) The LCD driver is stopped and segment and common driver outputs output the VDD level.
(c) An input of an external clock is inhibited and OSC2 enters the high-impedance state.
(d) The display data and operation mode before execution of the power save command are held.
(e) All LCD driver voltages are fixed to the VDD level.

The power save mode is cancelled by entering either the Display ON command or the Display All Points OFF command (display operation state). When external voltage driver resistors are used to supply the LCD driver voltage level, the current through them must be cut off by the power save signal.
If an external power supply is used, it must be turned OFF using the power save signal in the same manner and voltage levels must be fixed to the floating or VDD level.

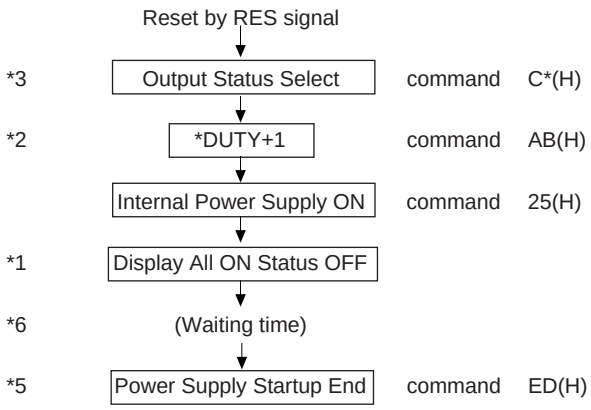
Sequence in the Power Save Status

Power Save and Power Save Clear must be executed according to the following sequence.
To give a liquid crystal driving voltage level by the externally-installed resistance dividing circuit, the current flowing in this resistance must be cut before or concurrently with putting the SED1560 series into the power save status so that it may be fixed to the floating or VDD level.
When using an external power supply, likewise, its function must be stopped before or concurrently with putting the SED1560 series ino the power save status so that it may be fixed to the floating or VDD level. In a configurationinwhich an exclusive common driver such as SED1630 is combined with the SED1560 series, it is necessary to stop the external power supply function after putting all the common output into non-selection level.

Power save sequence



Power save clear sequence



*1: In the power save sequence, the power save status is provided after the display all ON command. In the power save clear sequence, the power save status is cleared after the display all ON status OFF command.

*2 When the COMI pin is not used, it is not necessary to eneter the DUTY+1 command and DUTY+1 clear command.

*3 In the SED1562, it is not necessary to execute a command to decide an output status.

*4 The display ON command can be executed anywhere if it is later than the display all ON status OFF command.

*5 When internal power supply startup end command is not executed, current is consumed stationarily. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

*6 The waiting time depends on the Externally-installed capacitance C2 (refer to 4-35). After the waiting time shown in the above Graph 1, the power supply can be started surely.

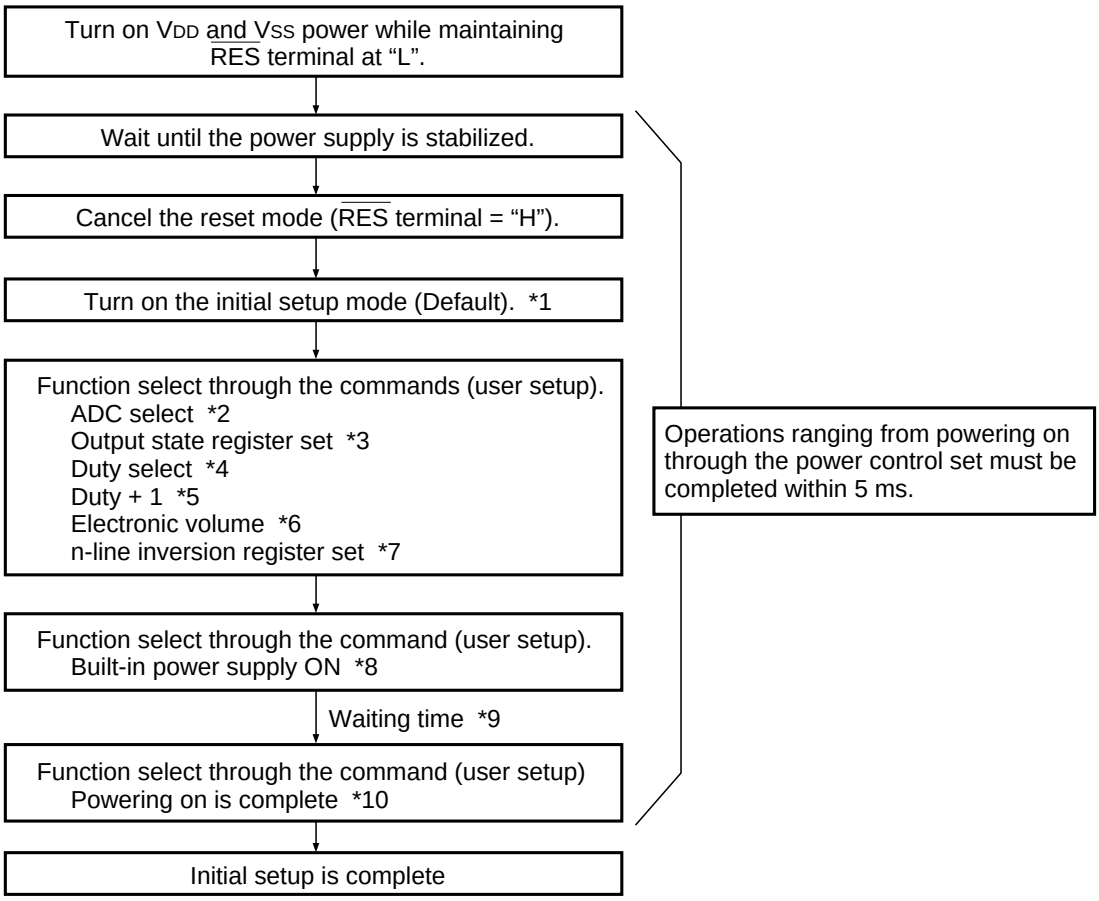
COMMAND DESCRIPTION – INSTRUCTION SETUP EXAMPLES

Instruction Setup Examples

Initial setup

Note: As power is turned on, this IC outputs non-LCD-drive potentials V_2 – V_3 from SEG terminal (generates output for driving the LCD) and V_1 –V_4 from COM terminal (also used for generating the LCD drive output). If charge remains on the smoothing capacitor being inserted between the above LCD driving terminals, the display screen can be blacked out momentarily. In order to avoid this trouble, it is recommended to employ the following powering on procedure.

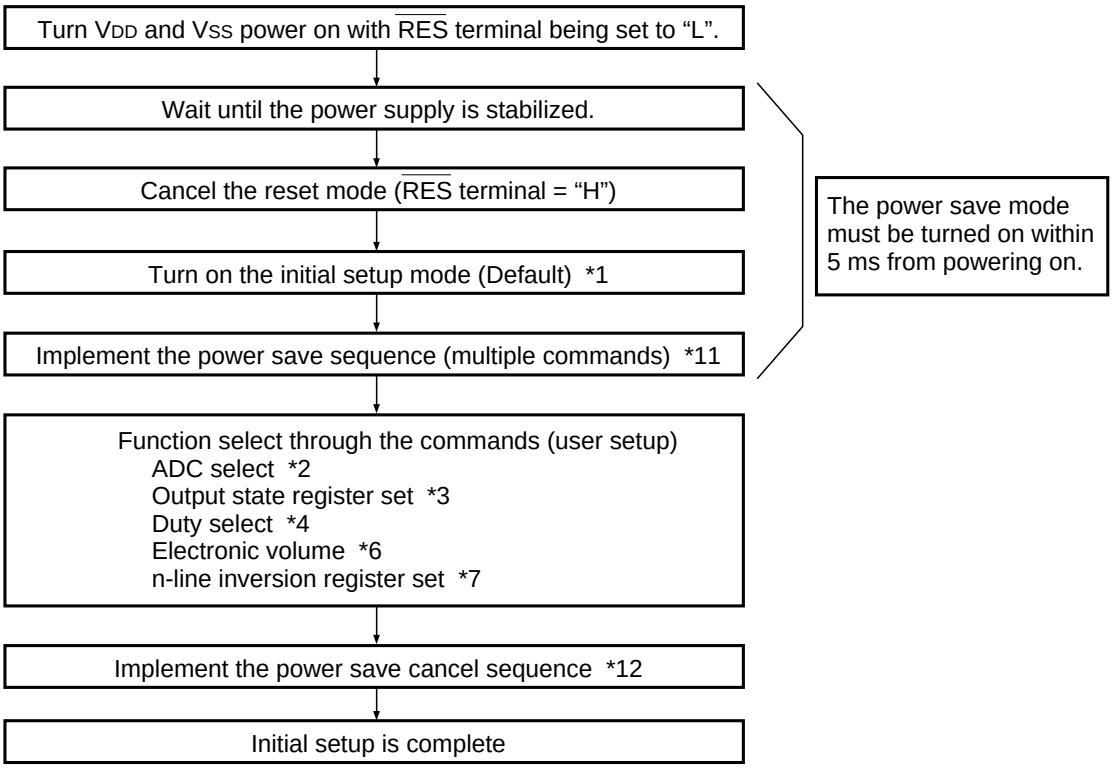
- **When the built-in power is used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned. Check them on the actual system.

Notes: *1: Refer to the "Reset Circuit" in the Function Description.
*2: Refer to the "ADC Select" in the Command Selection (8).
*3: Refer to the "Output State Register Set" in the Command Description (18).
*4: Refer to the "Duty Select" in the Command Description (11).
*5: Refer to the "Duty + 1" in the Command Description.
*6: Refer to the "Supply Circuit" in the Function Description and the "Electronic Volume Register Set" in the Command Description (21).
*7: Refer to the "n-line Inversion Register Set" in the Command Description (13).
*8: Refer to the "Built-in Power Supply ON/OFF" in the Command Description (21).
*9: Refer to the "Built-in Power Supply ON/OFF Sequence" in the Command Description.
*10: Refer to the "Built-in Power Supply ON Complete" in the Command Description (20).

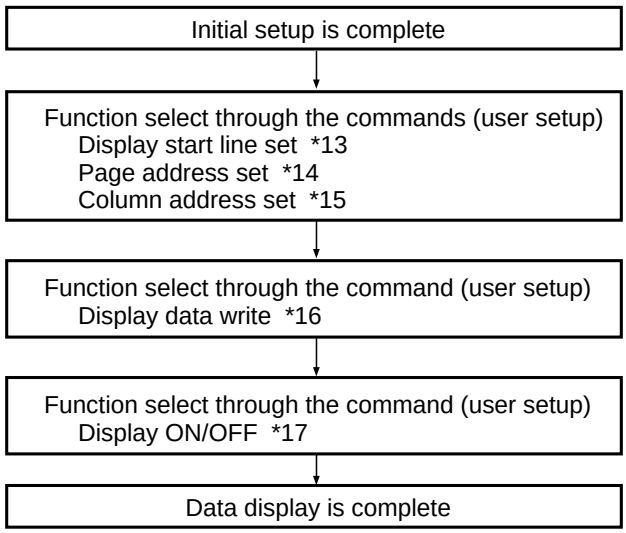
- **When the built-in power supply is not used immediately after the main power is turned on:**



* This duration of 5 ms depends on the panel characteristics as well as capacity of the capacitor concerned. Check them on the actual system.

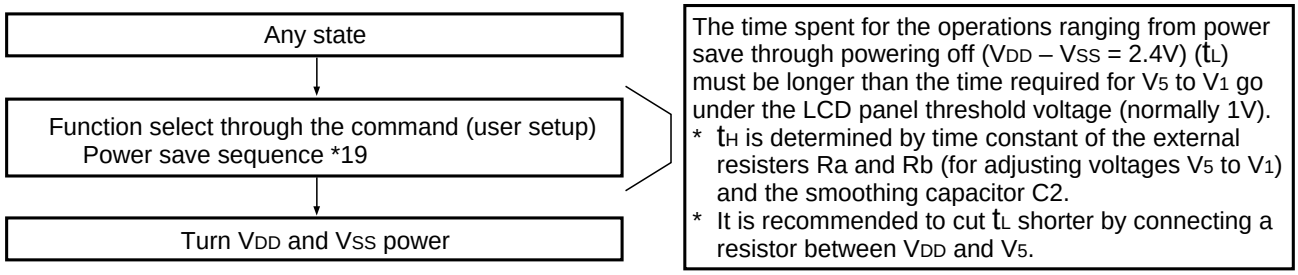
Notes: *1: Refer to the "Reset Circuit" in the Function Description.
*2: Refer to the "ADC Select" in the Command Description (8).
*3: Refer to the "Output State Register Set" in the Command Description (18)
*4: Refer to the "Duty Select" in the Command Description (11).
*6: Refer to the "Supply Circuit" in the Function Description and the "Electronic Volume Register Set" in the Command Description (21).
*7: Refer to the "n-line Inversion Register Set" in the Command Description (13).
*8: Refer to the "Built-in Power Supply ON/OFF" in the Command Description (19).
*11,12: You can select either the sleep mode or standby mode for the power save mode. Refer to the "Power Save (Multiple Commands)" in the Command Description (22).

- **Data Display**



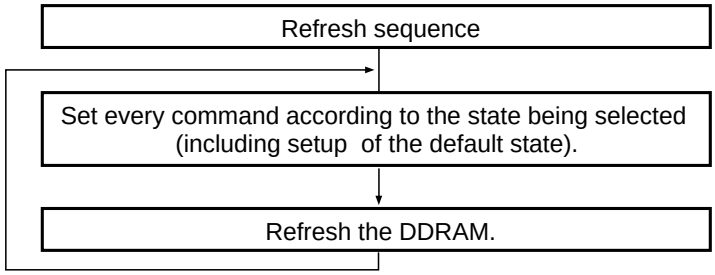
Notes: *13: Refer to the "Display Line Set" in the Command Description (2).
*14: Refer to the "Page Address Set" in the Command Description (3).
*15: Refer to the "Column Address Set" in the Command Description (4).
*16: Refer to the "Display Data Write" in the Command Description (6).
*17: Refer to the "Display ON/OFF" in the Command Description (1).
It is recommended to avoid the all-white-display of the display start data.

- **Powering Off** *18



Notes: *18: This IC functions as the logic circuit of the power supplies VDD – VSS, and used for controlling the driver of LCD power supplies VDD – V5. Thus, if power supplies VDD – VSS are turned off while voltage is still present on LCD power supplies VDD – V5, drivers (COM and SEG) may output uncontrolled voltage. Therefore, you are required to observe the following powering off procedure: Turn the built-in power supply off, then turn off the IC power supplies (VDD – VSS) only after making sure that potential of V5 – V1 is below the LCD panel threshold voltage level. Refer to the "Supply Circuit" in the Function Description.
*19: When the power save command is entered, you must not implement reset from RES terminal until VDD – VSS power are turned off. Refer to the "Power Save" in the Command Description.

- **Refresh**
It is recommended to use the refresh sequence on a regular basis. This sequence, however, must not be turned on as long as the initial setup, data display or powering off sequence is taking place.

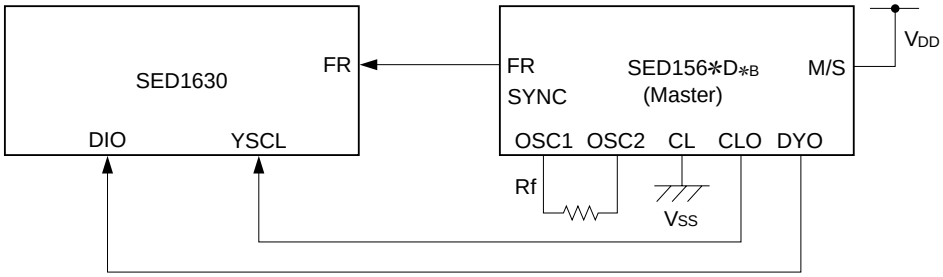


Connection between LCD drivers

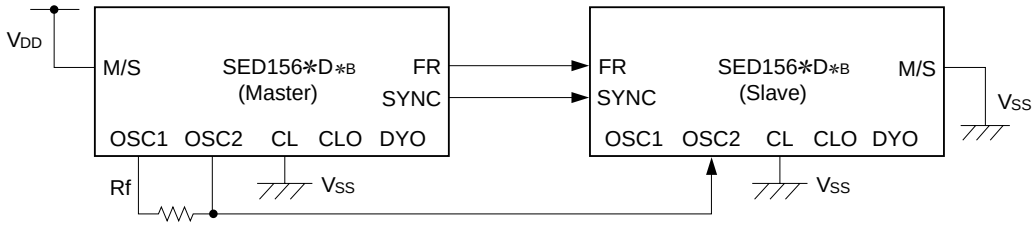
The LCD display area can be increased by using the SED1560 series in a multiple-chip configuration or with the SED1560 series special common driver (SED1630).

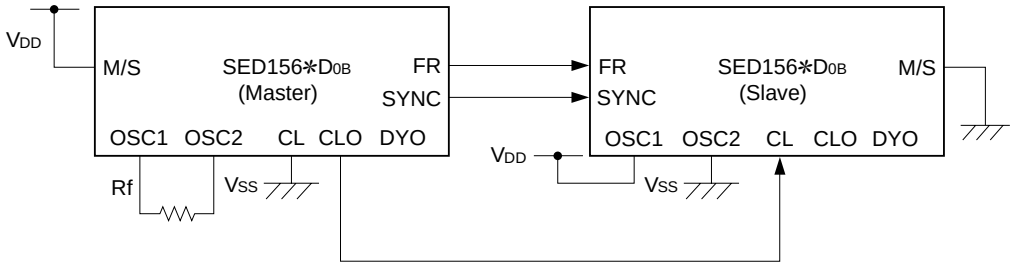
Application with external Driver

SED156✻D✻B–SED1630

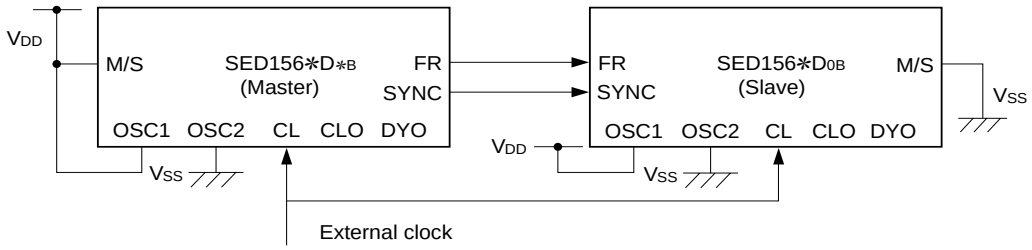


SED156✻D✻B–SED156✻D✻B
(when oscillator circuit is used)





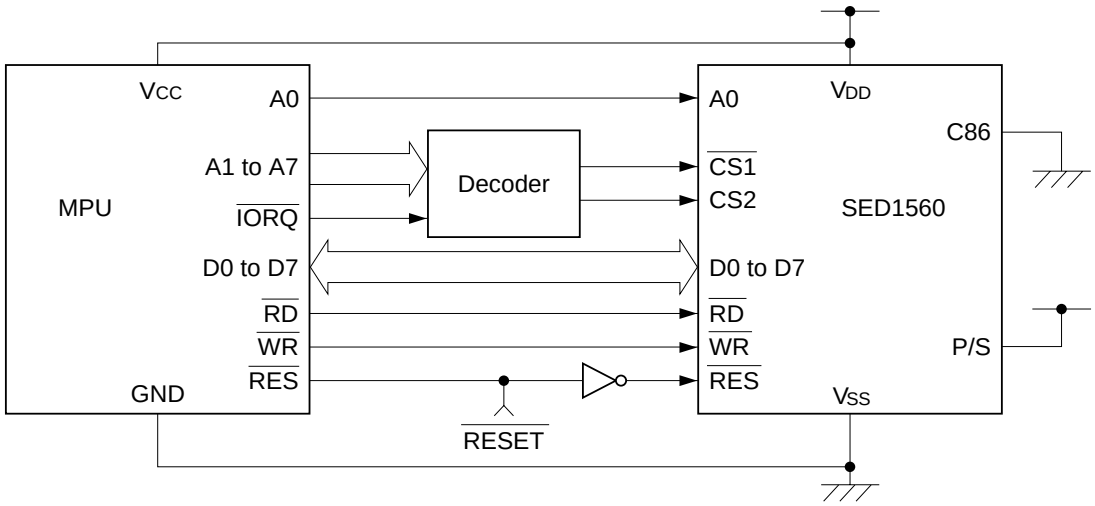
SED156✻D✻B–SED156✻D✻B (External clock)



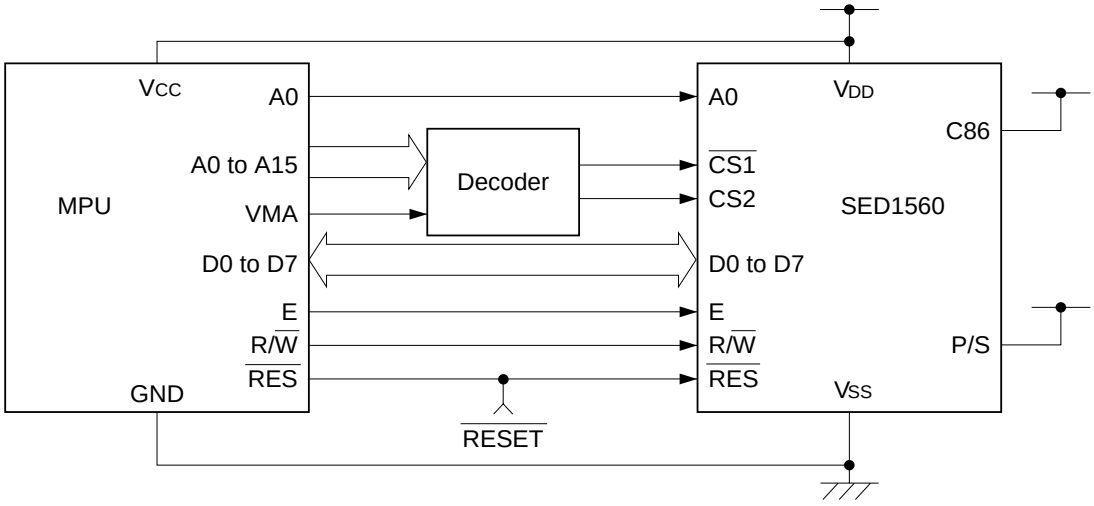
Microprocessor Interface

The SED1560 series interfaces to either 8080- or 6800-series microprocessors. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the SED1560 is controlled by the chip select signals from the microprocessor.

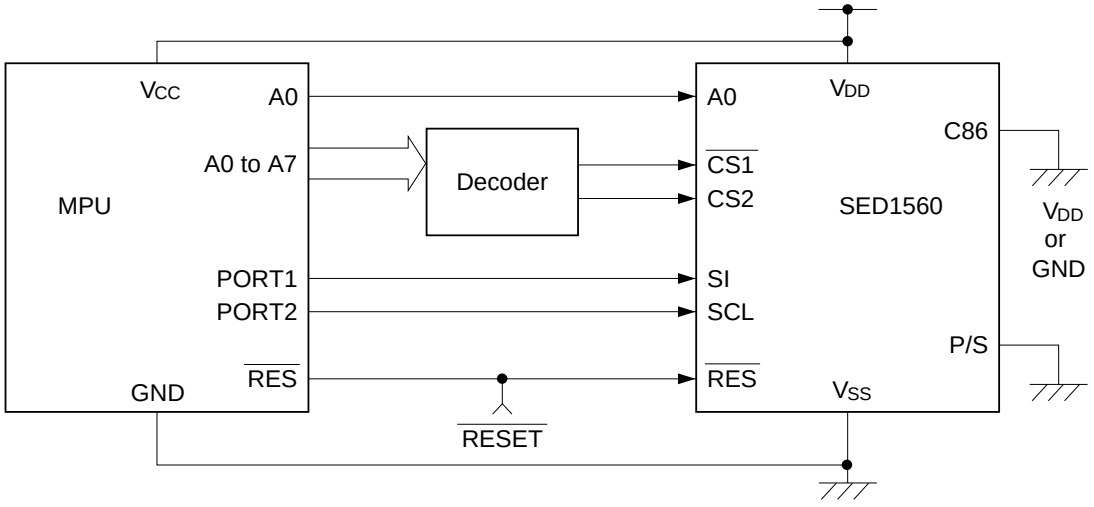
8080-series microprocessors



6800-series microprocessors

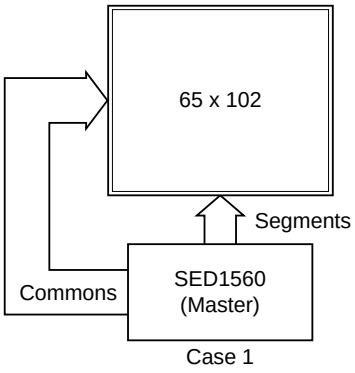


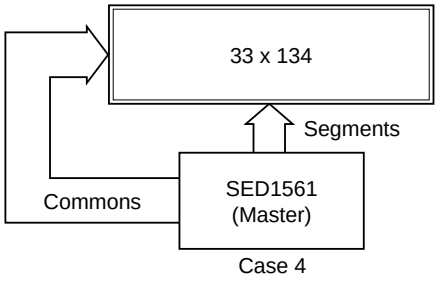
Serial interface

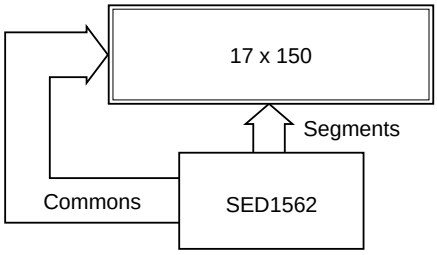


LCD Panel Interface Examples

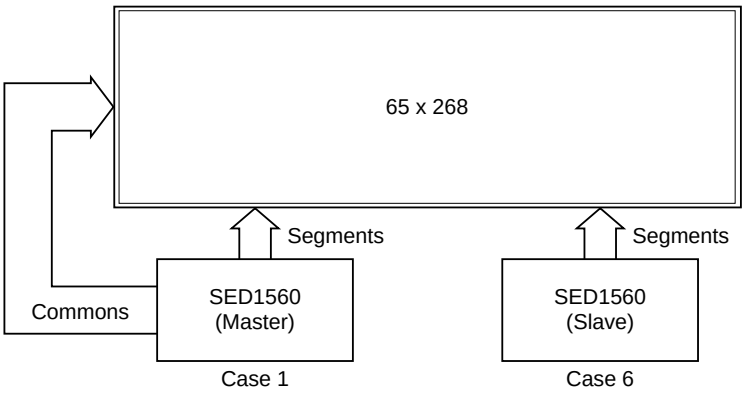
Single-chip configurations

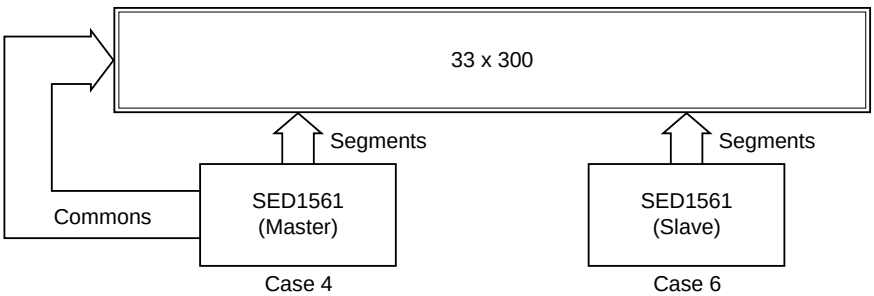




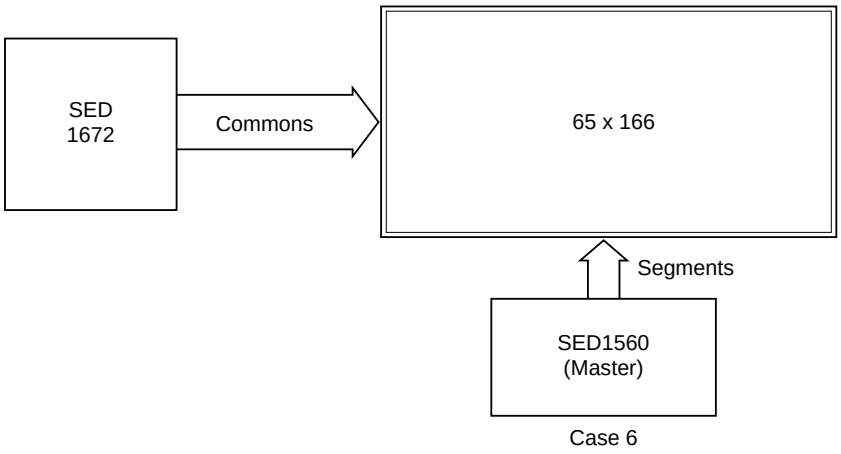


Multiple-chip configurations





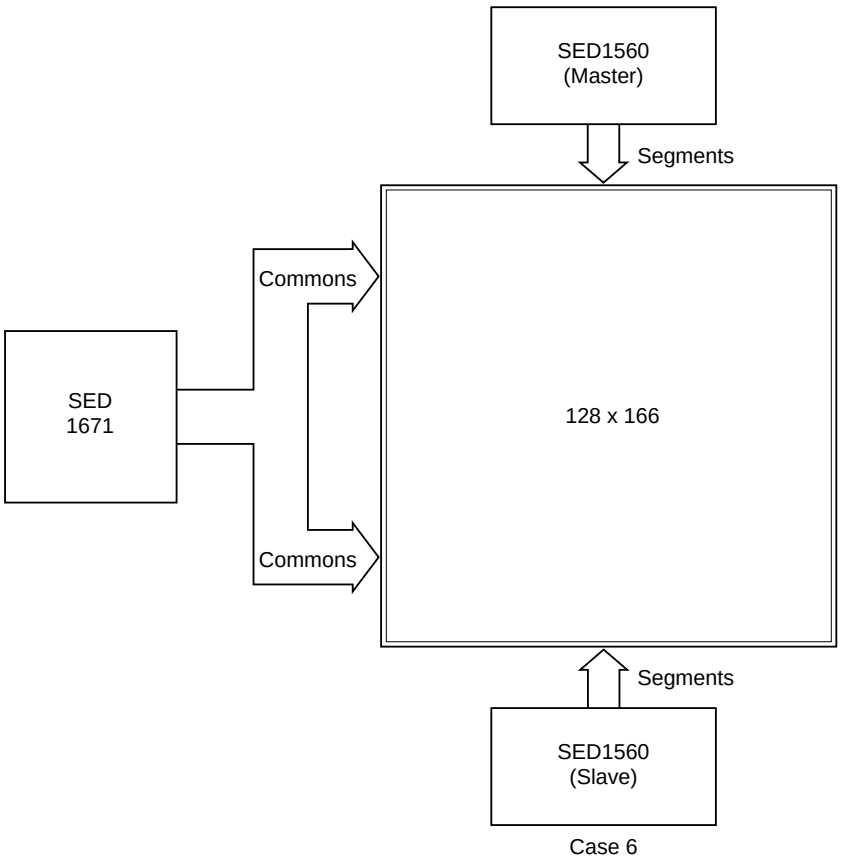
Special Common Driver Configurations



Case 6

* If an external amp circuit is configured, we recommend to use the SCI7660 and SCI7661.

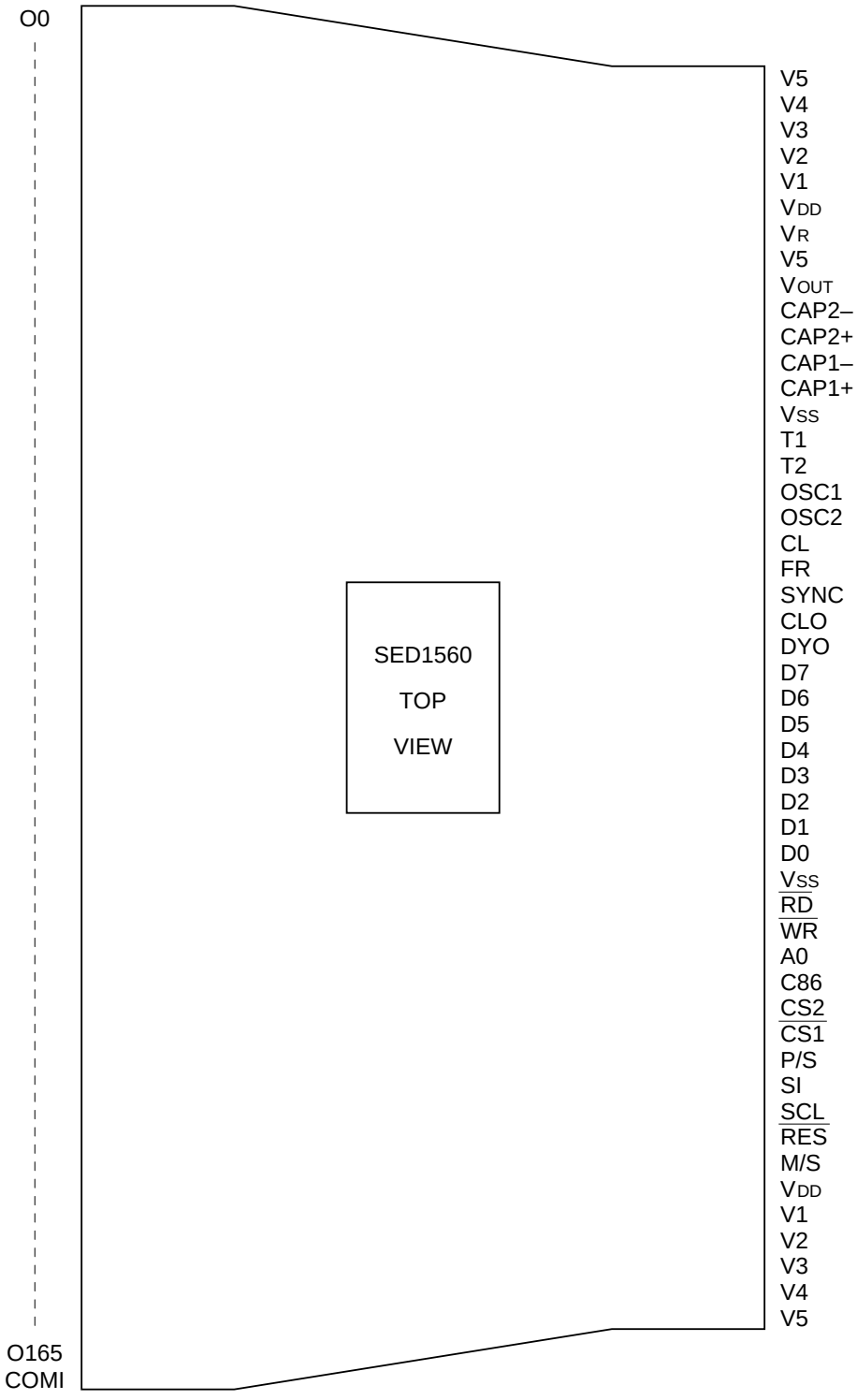
Case 6



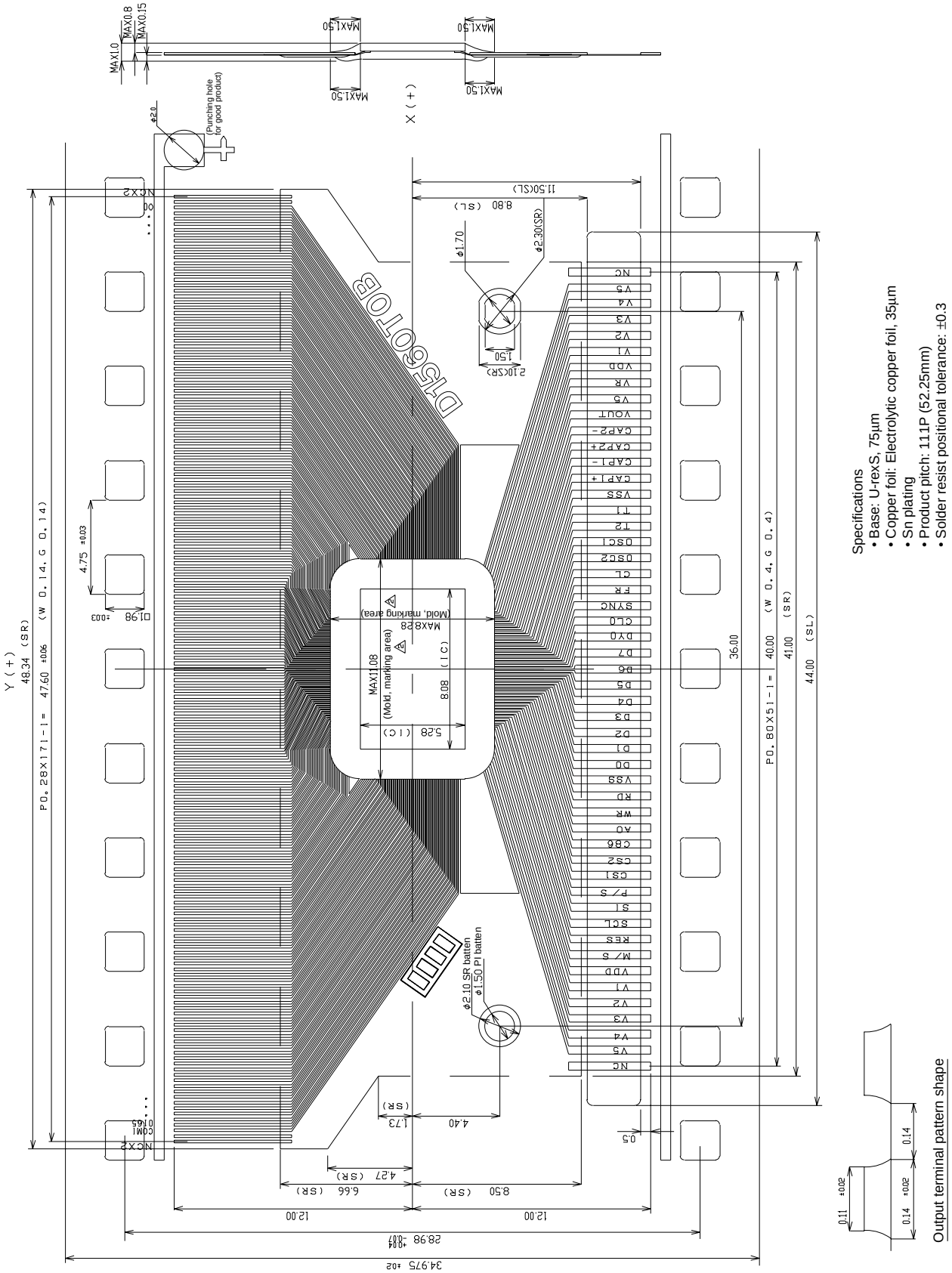
Case 6

SED1560T TAB Pin Layout

This drawing is not for specifying the TAB outline shape.



TCP DIMENSIONS (2 ways)



TCP DIMENSIONS (4 ways)